LINEARIZATION AND EFFICIENCY ENHANCEMENT TECHNIQUES FOR RF AND BASEBAND ANALOG CIRCUITS

A Dissertation

by

MOHAMED SALAH MOHAMED MOBARAK

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2010

Major Subject: Electrical Engineering

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ABSTRACT

Linearization and Efficiency Enhancement Techniques for RF and Baseband Analog Circuits. (December 2010)

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Chair of Advisory Committee: Dr. Edgar Sanchez-Sinencio

High linearity transmitters and receivers should be used to efficiently utilize the available channel bandwidth. Power consumption is also a critical factor that determines the battery life of portable devices and wireless sensors. Three base-band and RF building blocks are designed with the focus of high linearity and low power consumption.

An architectural attenuation-predistortion linearization scheme for a wide range of operational transconductance amplifiers (OTAs) is proposed and demonstrated with a transconductance-capacitor (Gm-C) filter. The linearization technique utilizes two matched OTAs to cancel output harmonics, creating a robust architecture. Compensation for process variations and frequency-dependent distortion based on Volterra series analysis is achieved by employing a delay equalization scheme with on-chip programmable resistors. The distortion-cancellation technique enables an IM3 improvement of up to 22dB compared to a commensurate OTA without linearization. A

proof-of-concept lowpass filter with the linearized OTAs has a measured IM3 < -70dB and 54.5dB dynamic range over its 195MHz bandwidth.

Design methodology for high efficiency class D power amplifier is presented. The high efficiency is achieved by using higher current harmonic to achieve zero voltage switching (ZVS) in class D power amplifier. The matching network is used as a part of the output filter to remove the high order harmonics. Optimum values for passive circuit elements and transistor sizes have been derived in order to achieve the highest possible efficiency. The proposed power amplifier achieves efficiency close to 60% at 400 MHz for -2dBm of output power.

High efficiency class A power amplifier using dynamic biasing technique is presented. The power consumption of the power amplifier changes dynamically according to the output signal level. Effect of dynamic bias on class A power amplifier linearity is analyzed and the results were verified using simulations. The linearity of the dynamically biased amplifier is improved by adjusting the preamplifier gain to guarantee constant overall gain for different input signal levels.

DEDICATION

To the memory of my mother

To my father

To my brothers and sisters

To my wife

For all their love and support

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I would like to express my deep gratitude to my advisor, Dr. Edgar Sanchez-Sinencio, for his guidance and support throughout the course of my research. His valuable comments and encouragement made this research possible and I deeply appreciate his immediate help in solving many problems that I have faced during my studies.

I would like to thank Dr. Jose Silva-Martinez for being a member of my committee and for his valuable input, suggestions and comments especially on the Gm-C filter linearization project. I also would like to thank my committee members Dr. Prasad Enjeti and Dr. Mahmoud El-Halwagi for their time and valuable comments.

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I enjoyed the company and discussions with many friends including Faramarz Bahmani, Faisal Hussien, Marvin Onabajo, Mohamed Elsayed, Mohammed Abdul-Latif, Mohamed El-Nozahi, Ahmed Amer, Ehab Sobhy, Ahmed Helmy, Ramy Saad, Aymen Ameen, Ahmed Ragab, and Jason Wardlaw. Their help and encouragement was an essential factor for me during my study.

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CHAPTER I

INTRODUCTION

1.1 Motivation

Internet, smart phones, and global positioning system (GPS) navigation have become an essential part of our daily lives. Advances in communication technologies enabled the integration of multiple features to a single device, for example mobile phones are used to transfer videos as well data over the internet and they can be used as GPS navigation devices beside their main use of transmitting voice signals. Moreover, many new applications that utilize wireless bandwidth have recently emerged such as satellite communications which is being used to provide important services to remote locations. These advances in wireless systems led to a very crowded wireless spectrum. The amount of data required to be transmitted over the wireless connections has increased significantly while the available bandwidth is very limited.

New techniques must be used in order to allow high data rate transmission over the available bandwidth and to extract the weak signal received in the presence of strong interference. Low noise receivers are necessary to distinguish the received signal from the noise level. On the other hand, high linearity receiver is required to minimize the effect of the interfering signals over the desired signal.

This dissertation follows the style of *IEEE Journal of Solid-State Circuits*.

Low power operation is also desired for mobile transceivers. In some applications, such as sensor networks or implantable medical sensors, power consumption is a crucial factor when designing the transceiver building blocks. The goal of this research is to develop new circuits and techniques to build high linearity receivers and high efficiency transmitters. While the noise contribution of the first block in wireless receiver is the most critical compared to the rest of the receiver, the non-linearity of base-band blocks in wireless receivers is the dominant source of non-linearity in the whole receiver. On the transmitter side, the power amplifier efficiency is one of the major factors that determine the whole transmitter power consumption. New circuit techniques has been proposed for the following base-band and RF blocks

1) High linearity base-band filter using attenuation-predistortion linearization technique for the use in wide-band receivers.
2) High efficiency class D power amplifier for low output power applications.
3) High efficiency class A power amplifiers with dynamic bias control for high linearity transmitters in applications that involve envelope modulated signal transmission.

1.2 Dissertation Organization

Chapter II discusses the development of new architectural technique for the linearization of operational transconductance amplifiers (OTA) that is used as a part of OTA-C filters. Since there is an increasing demand of higher data rate and consequently

wider channel bandwidth, the high frequency effects associated with the proposed techniques is analyzed and frequency compensation scheme is proposed. Tradeoff associated with the proposed techniques, effect of process-voltage-temperature (PVT) variations is also provided in details. Measurement result of a standalone operational transconductance amplifier is presented and compared to a reference transconductance amplifier fabricated on the same chip that doesn't utilize the proposed linearization technique. Results of second order low pass filter that is build using the proposed OTA is also given.

Design of high efficiency switching power amplifiers is addressed in Chapter III with a description of the advantages and the disadvantages of different power amplifier classes. Efficiency analysis of class D power amplifier is provided and optimization of class D efficiency for low power applications is given. The high efficiency operation is verified with the measurement results of a 400 MHz class D power amplifier.

Chapter IV presents a study of class A power amplifier dynamic biasing and its effect on the amplifier linearity. High efficiency and high linearity operation of class A power amplifier using dynamic biasing is proposed. Linearity enhancement using dynamic bias is analyzed and measurement results for dynamically biased class A amplifier is provided.

Conclusions are summarized in Chapter V and possible areas of future work are also presented.

CHAPTER II

ATTENUATION-PREDISTORTION LINEARIZATION OF CMOS OTAS FOR OTA-C FILTER APPLICATIONS*

2.1 Introduction

Operational transconductance amplifiers (OTAs) are essential elements of transconductance-capacitor (G_m-C) filters [1]-[3], ΔΣ modulators [4], gyrators, variable-gain amplifiers, and negative-resistance elements. Compared to their active-RC counterparts, G_m-C filters enable low-power operation and tuning of the filter characteristics at higher frequencies, but are less linear. Tunable active-RC filters are suitable for low-frequency applications (e.g. <20MHz in [5]); however, extending their use to higher frequencies would require significantly more power. On the other hand, OTA-based filters in wireless receivers and continuous-time (CT) ΔΣ analog-to-digital converters (ADCs) increasingly mandate good linearity at higher frequencies. These applications typically require highly linear OTAs with third-order inter-modulation (IM3) distortion better than -60dB. Further advances in high-frequency G_m-C filters with SNDRs over 50dB are also desirable for channel selection/equalization in multi-Gbps portable data communication devices [3], and for possible application in next generation analog-to-information receivers with dynamic range > 90dB in 200MHz bandwidth [6].

Viable high-frequency G_m-C filter solutions were presented in [1] and [7] with 3-dB frequencies at 275MHz and 184MHz, respectively. The topology reported in [1] has low noise, limited linearity, and a pseudo-differential realization prone to low power supply rejection ratio (PSRR). The filter in [7] achieves high linearity with relatively low power but higher noise. Trade-offs between linearity, noise, power, and operating frequency are common and have been incorporated into figures of merit (FOMs) such as in [8] and [9]. The filter cutoff frequency tuning range can also be incorporated into a FOM [10], which aids in the comparison of G_m-C filters for applications in which reconfigurability is important; e.g. wide tuning capability such as the 25:1 range in [10] is beneficial in multi-standard receivers. Recent works also address alternative filter structures such as the source-follower-based approach [11] and performance improvement of typical OTA topologies [12].

A popular linearization approach is to cross-couple two transconductors, theoretically cancelling certain harmonics at specific bias conditions over a limited frequency range. Non-linearity cancellation with two devices in parallel has been successfully extended to narrow-band RF transconductors in [13]. A typical cross-coupled OTA contains two paths; each having different transconductance and the same amount of harmonic distortion as illustrated by the block diagram in Fig. 2.1. When cross-coupled, the equal harmonics cancel under ideal conditions and the effective transconductance is the difference between the two paths. The frequency dependence of this approach has been analyzed with Volterra series in [14], in which the analytical expressions are correlated with measurement results. Process-voltage-temperature (PVT)

variations, high-frequency effects, and device modeling inaccuracies will create unforeseen mismatches between the two amplifiers. Therefore, precision tuning of bias currents/voltages is typically required. Signal attenuation can be also used to linearize the amplifier in the expense of gain reduction. Attenuation and cross-coupling has been combined for the low-noise amplifier in [15], in which distortion cancellation is restricted to third-order non-linearities with feedforward path and precise off-chip input attenuation. Accurate modeling of frequency-dependent distortion characteristics on the MOSFET device level is presented in [16].

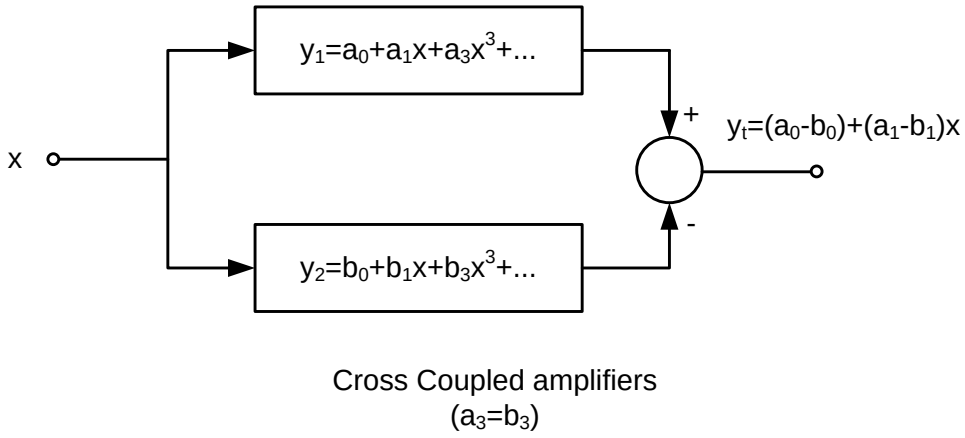


Fig. 2.1. Block diagram of cross coupled amplifiers.

For a source coupled differential pair biased by a current source I_{DC}, the differential output current is expressed in terms of the differential input voltage v_d as $I_o = v_d \sqrt{\beta I_{DC} - \beta^2 v_d^2 / 4}$, where $\beta = \mu_0 C_{ox} W/L$, μ_0 is the electron mobility, C_{ox} is the gate oxide per unit area, W is the transistor width, and L is the transistor length. The bias

current of the differential pair can be adjusted dynamically in order to linearize the OTA [17]. If the bias current I_{DC} is adjusted such that $I_{DC} = I_{DC0} + (\beta/4)v_d^2$, then the output current is linearly proportional to the input differential voltage v_d and it is given by $I_o = v_d\sqrt{\beta I_{DC0}}$. However, in deep submicron technologies, other third order nonlinearities arise from short channel effects which were neglected in the previous analysis and thus finite third order nonlinearities will not be cancelled by this technique.

The proposed methodology is an architectural solution that achieves up to 22dB IM3 improvement over an identical non-linearized OTA design at frequencies as high as 350MHz. It can be generalized to fully-differential topologies which offer higher PSRR and common-mode rejection ratio (CMRR). Since the maximum frequency is mainly limited by process parasitics and OTA performance, the approach shows promise of exceeding 350MHz bandwidth in future nanoscale CMOS processes. Robust linearization over a wide frequency range demands a mechanism to correct for high-frequency effects and PVT variations, for which a digital programmability scheme is proposed.

2.2 Attenuation-Predistortion Linearization Methodology

Signal attenuation at the OTA input [14] reduces the effective transconductance and decreases the SNR. Alternatively, distortion cancellation by means of cross-coupled differential pairs results in increased power consumption and noise proportional to the transistor parameters in the additional path. Since the extra differential pair normally has less transconductance than the main pair, the effective transconductance is reduced by

10-50%. However, both transistor pairs should have the same third-order non-linearity, which translates into different transistor sizes and bias currents for each pair. As a result, the cross-coupling technique is sensitive to PVT variations and restricted to narrow frequency ranges. Another common method to linearize a transistor having transconductance g_m is to add a degeneration resistor R_{sd} at the source [14], which makes the third-order harmonic distortion proportional to the factor $1/(1+g_mR_{sd})^3$. Nonetheless, large degeneration resistance results in higher input-referred noise, lower transconductance, and less voltage headroom. The effective transconductance (g_{msd}) and the input-referred noise (v^2_{nsd}) with resistive source degeneration are given by

$$g_{msd} = \frac{g_m}{1+g_mR_{sd}} \quad , \quad v^2_{nsd} \approx \frac{4KT}{g_m}\left(\frac{2}{3}+g_mR_{sd}\right), \tag{2.1}$$

where the noise coefficient γ was approximated as 2/3. For example, using a degeneration factor $g_mR_{sd} = 2$ will ideally result in IM3 improvement of approximately 29dB, an input-referred noise power increase by a factor of 4, and a decrease of the transconductance to one third of its original value. But based on simulations of the OTA from this work with $g_mR_{sd} = 2$, the expected IM3 improvement would be 25.2dB with an associated noise power increase of more than 9 times.

The proposed attenuation-predistortion [18] method is independent of OTA topology and involves cancellation of all distortion components except those from secondary effects at high frequencies. It can be used in conjunction with other circuit-level linearization techniques internal to the OTA, such as source degeneration or cross-coupling.

2.2.1 Single-Ended Circuits

The proposed linearization scheme is illustrated in Fig. 2.2 where the non-linear system is linearized by subtracting the harmonics created in an identical system. Fig. 2.3 depicts the single-ended architecture that contains an auxiliary branch with an OTA having identical dimensions, DC bias, and AC common-mode conditions as in the main path to generate the distortion components required for cancellation.

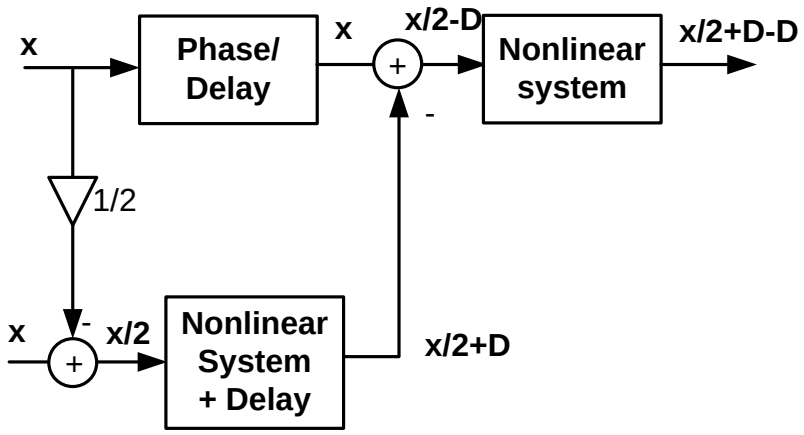


Fig. 2.2. Block diagram of the proposed attenuation-predistortion technique.

An important advantage of identical paths is robustness to PVT variations because of optimal device matching obtainable from proper layout. In this scheme, it is avoided to base the distortion cancellation on branches with different transconductor device dimensions or bias conditions, which would degrade matching accuracy. But even with minimized mismatches, non-linearities are particularly frequency-dependent at high frequencies and remain sensitive to PVT variations as established in Section 2.5.

Hence, the proposed linearization method involves variable resistors to tune performance and counteract high-frequency degradation as well as PVT variations. Either a resistive or capacitive divider can form the attenuator at the input of the auxiliary path; however, resistors add more noise.

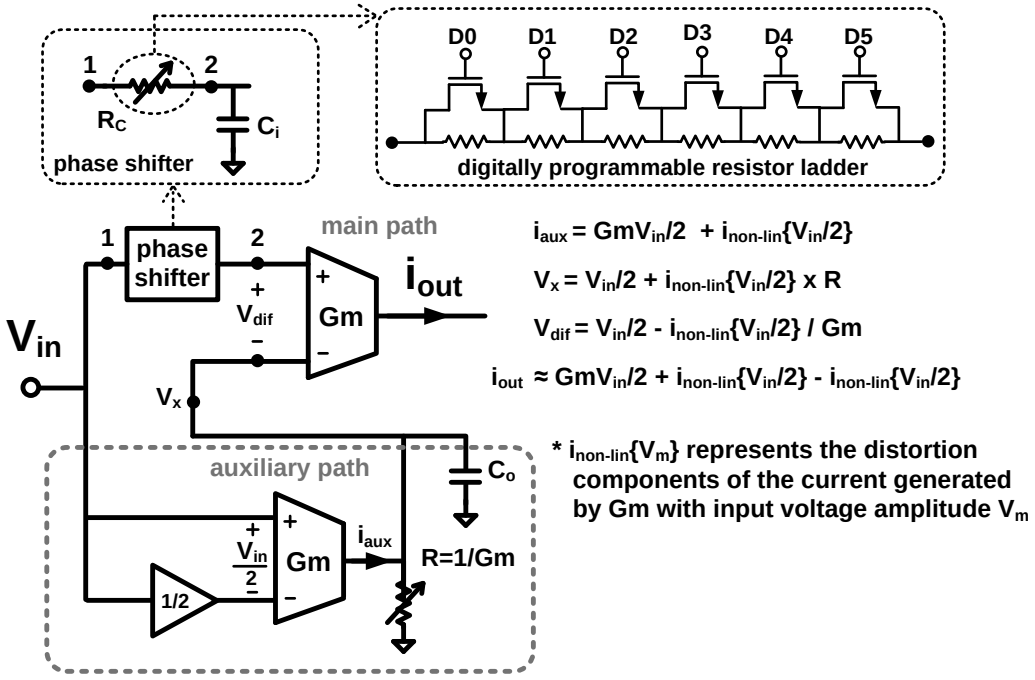


Fig. 2.3. Attenuation-predistortion linearization scheme for single-ended circuits.

Distortion cancellation in the single-ended case requires $G_m \times R = 1$, which is ascertained by the following analysis. For a certain input voltage amplitude V_m, the output current can be divided into a linear part $i_{lin}\{V_m\} = G_m \times V_m$ and a non-linear part $i_{non\text{-}lin}\{V_m\} = g_{m2} \times V_m^2 + g_{m3} \times V_m^3 + \ldots$, where g_{m2}, g_{m3},… are Taylor series coefficients of the transconductance. The differential input of the main OTA is: $V_{dif} = V_{in} - [\, V_{in}/2 + i_{non\text{-}lin}\{V_{in}/2\}/G_m \,] = V_{in}/2 - i_{non\text{-}lin}\{V_{in}/2\}/G_m$. Under ideal conditions, the distortion

generated in the auxiliary path, $-i_{non\text{-}lin}\{V_{in}/2\}$, cancels out the distortion in the main voltage-to-current conversion. In practice, distortion caused by non-linearities at the output of the auxiliary OTA and high-frequency effects introduces some finite uncancelled distortion. Capacitor C_o represents the lumped output capacitance of the auxiliary OTA, input capacitance of the main OTA, and layout parasitics. Resistor R_c of the phase shifter and equivalent input capacitance C_i provide 1^{st}-order frequency compensation, creating a pole to equalize the phase shift between the main and auxiliary paths. Compensation is necessary at high frequencies because parasitic capacitance C_o at the negative input terminal of the main OTA creates a pole with resistor R in the auxiliary path.

2.2.2 Fully-Differential Circuits

A conceptual diagram of the proposed linearization approach for a fully-differential transconductor (G_m) and the corresponding circuit diagram are displayed in Fig. 2.4 and Fig. 2.5 respectively. In the fully-differential case, attenuation factors at the input of the transconductors are chosen such that it can be realized with floating-gate devices as described in Section 2.4.1.

As discussed in [14], [19] and [20], the inherent input attenuation with floating-gate stages enhances the OTA linearity. The distortion cancellation principle is the same as in the single-ended case, but different conditions must be satisfied for fully-differential implementation, which are explained in Sections 2.2.3 and 2.4.1 with regards to the attenuation ratios.

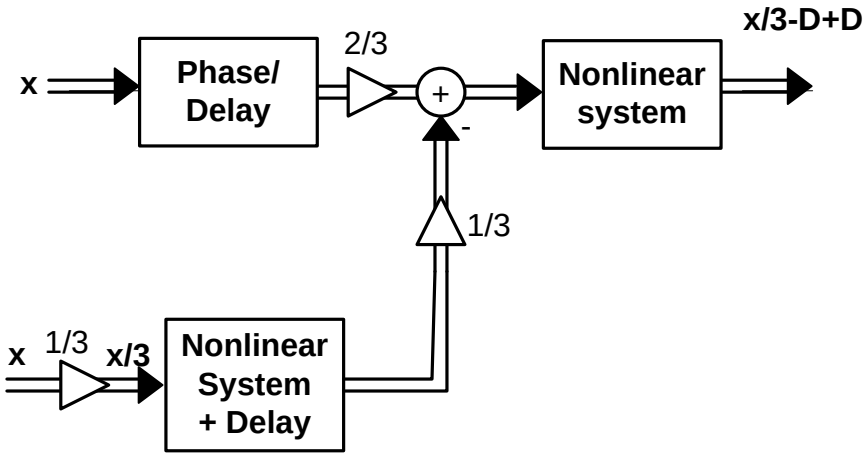


Fig. 2.4. Block diagram of the fully differential implantation of the attenuation-predistortion technique.

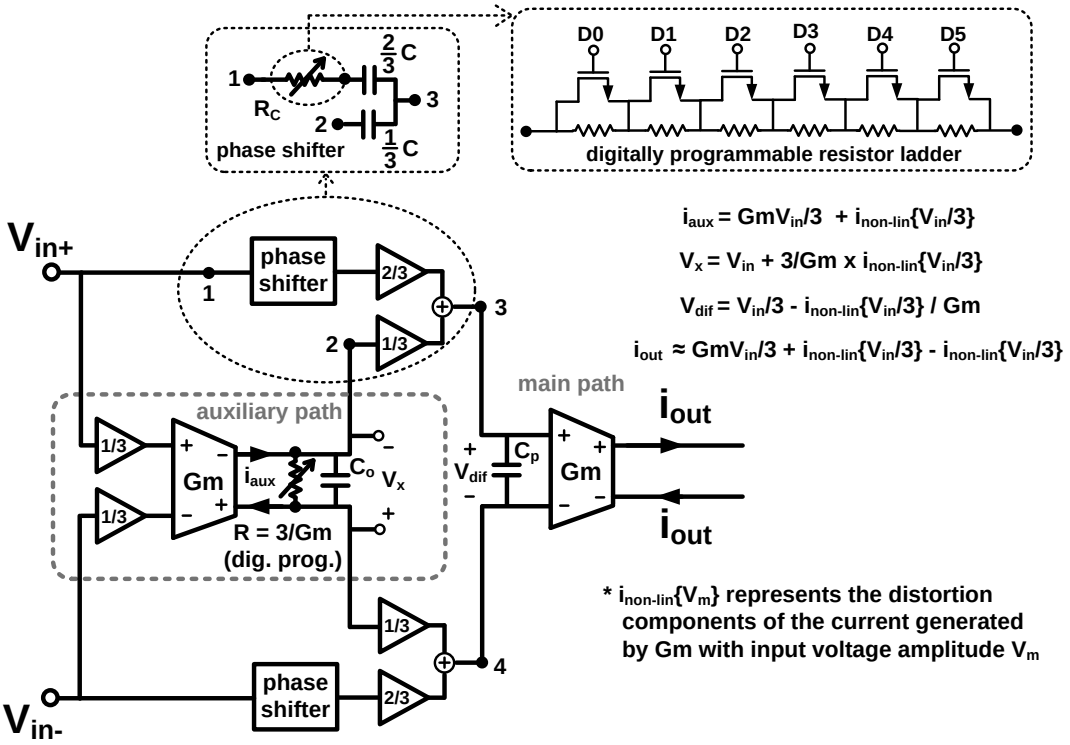


Fig. 2.5. Attenuation-predistortion linearization for fully-differential circuits.

By selecting an input attenuation ratio of 1/3 and voltage gain of 3 in the auxiliary branch ($G_m \times R = 3$), the signal amplitude V_x is equal to V_{in} plus three times the distortion components caused by the non-linear current $i_{non\text{-}lin}\{V_{in}/3\}$ from the transconductor with input amplitude of $V_{in}/3$. In the main path, the effective differential OTA input is: $V_{dif} = 2V_{in}/3 - V_x/3 = 2V_{in}/3 - [\ V_{in} + 3 \times i_{non\text{-}lin}\{V_{in}/3\}/G_m\ ] / 3 = V_{in}/3 - i_{non\text{-}lin}\{V_{in}/3\}/G_m$. Thus, the differential signal contains the attenuated input signal and the inverse of the distortion generated by the identical G_m in the auxiliary branch for distortion cancellation during the voltage-to-current conversion in the main path. Ideally, the distortion components are canceled by the equal and opposite terms from the predistortion of the differential input signal except for negligible higher-order components. C_o in Fig. 2.5 represents the equivalent differential capacitance of all parasitic capacitances at the output of the auxiliary OTA and C_p is the differential equivalent of the parasitic capacitances at the input of the main OTA. Expressions for optimum distortion cancellation at high frequencies are provided in Section 2.3.

Linear RC phase shifter networks are chosen for the frequency compensation implementation in order not to affect the cancellation scheme. Resistors R and R_c are tuned with 6-bit resolution to compensate for mismatches/PVT variations. The phase shifter block is utilized to equalize the delay from the input to summing nodes 3 and 4 in Fig. 2.5. Furthermore, the phase shifter enables optimization of the non-linearity cancellation based on high-frequency effects.

2.2.3 Scaling of Attenuation Ratios

Depending on application-specific requirements, the design parameters in the attenuation-predistortion linearization approach can be selected to adjust the voltage swings and the effective transconductance. Fig. 2.6 shows the fully-differential attenuation-predistortion linearization scheme, where frequency compensation and parasitic capacitors have been omitted for simplicity.

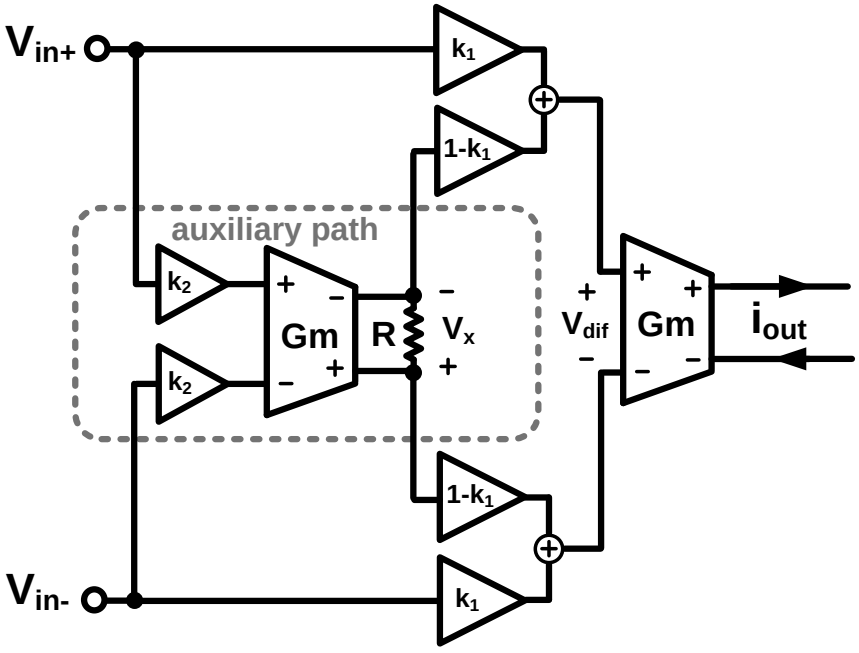


Fig. 2.6. Low-frequency model for the fully-differential attenuation-predistortion scheme.

The following analysis assumes floating-gates as a practical attenuator implementation choice under the constraint that factors k_1 and $(1-k_1)$ are related as elaborated upon in Section 2.4.1, but less restrictive types of attenuators could also be

used. As mentioned before, the output current i_o of an OTA due to an input voltage V_m can be modeled as having a linear and a non-linear part: $i_o = G_m V_m + i_{non\text{-}lin}\{V_m\}$. Ignoring high-frequency and secondary effects, the following relation can be written:

$$\begin{aligned} i_{out} \approx\ & G_m\left(k_1-(1-k_1)k_2G_mR\right)V_{in} - (1-k_1)G_mR\cdot i_{non\text{-}lin}\{k_2V_{in}\} \\ & + i_{non\text{-}lin}\{\left(k_1-(1-k_1)k_2G_mR\right)V_{in}\} \end{aligned}, \qquad (2.2)$$

where: $i_{non\text{-}lin}\{k_2V_{in}\}\cdot R(1-k_1) \ll (k_1-(1-k_1)k_2G_mR)V_{in}$ is assumed in the approximation. To cancel the distortion, the following conditions should hold:

i) The auxiliary and main OTAs should have the same effective input voltage amplitudes such that an identical distortion is created at their respective outputs.

ii) The gain in the auxiliary path must ensure that the distortion through this signal path reaches the output of the main OTA with a gain of -1.

iii) The internal signal swings should be bounded, i.e.:

$$k_2G_mR \le 1 \qquad (2.3)$$

Applying conditions i) and ii), cancellation of the non-linear terms in (2.2) requires:

$$(1-k_1)G_mR = 1 \quad , \quad k_2 = k_1/2 \qquad (2.4)$$

Consequentially, the effective transconductance with linearization is given by

$$G_{meff} = \left(k_1-(1-k_1)k_2G_mR\right)G_m = (k_1/2)G_m = k_2G_m \qquad (2.5)$$

Condition iii) depends on the application and is not always necessary. Cancellation of distortion with the proposed technique requires weakly non-linear operation in the auxiliary branch, which is ensured by limiting the signal swing with this condition. The example that is presented in Fig. 2.5 was derived with $k_2G_mR = 1$,

ensuring that the signal swing at the output of the auxiliary OTA is the same as at its input. This choice was made to maintain the same maximum input voltage swing as the initial OTA without saturating the OTA in the linearization path. If the specified input signal is k_2G_mR times below the OTA saturation level, then k_2 can be increased accordingly to obtain $k_2G_mR > 1$ and higher effective transconductance based on (2.5). But, this choice is only permissible if a reduction of the maximum input swing by k_2G_mR can be tolerated, which would imply a reduction in the dynamic range. Typically, choosing $k_2G_mR = 1$ is advantageous to maintain the same maximum input voltage swing as the original OTA after linearization. Selection of $k_1 = 2/3$ and $k_2 = 1/3$ results in the highest effective transconductance that can be achieved in (2.5) based on the above conditions while also satisfying the attenuation factor relationships in the floating-gate devices (Section 2.4.1) with identical signal swings at the input and output of the auxiliary OTA ($k_2G_mR = 1$). Hence, $G_mR = 3$ under the stated conditions.

2.3 Volterra Series Analysis

The preceding expressions are valid at low frequencies and give insight into the conditions to cancel total distortion when secondary effects are negligible. Volterra series analysis [21] is used to find the optimum compensation resistor value for linearization at high frequencies. Employing a 3rd-order model of transconductor non-linearity, the simplified model of the proposed attenuation-predistortion linearization technique is shown in Fig. 2.7. In this analysis, g_{m1} represents the linear transconductance and g_{m3} the third-order component. Resistor (R_c) compensates for

high-frequency linearity degradation by equalizing the delays in the main and auxiliary paths.

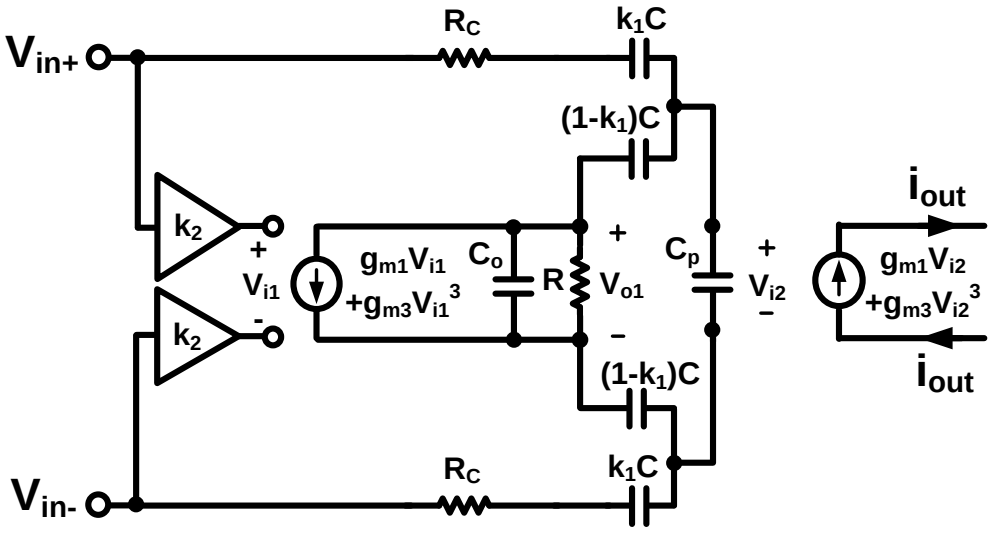


Fig. 2.7. Non-linear model for fully-differential attenuation-predistortion cancellation.

The differential voltage $V_{i2}(t)$ at the input of the main OTA is given by

$$V_{i2}(t) = -\left(g_{m1}k_2V_{in}(t) + g_{m3}[k_2V_{in}(t)]^3\right)\cdot\frac{R\cdot(1-k_1)}{1+2C_p/C}\cdot\frac{1+j\omega Ck_1R_c}{1+j\omega b-c\omega^2} + V_{in}(t)\cdot\frac{k_1}{1+2C_p/C}\cdot\frac{1+j\omega C(1-k_1)R/2+j\omega C_oR}{1+j\omega b-c\omega^2}, \quad (2.6)$$

where :

$$b = \frac{C(k_1/2)(1-k_1)(R+2R_c)+2k_1C_pR_c+(1-k_1)C_pR}{1+2C_p/C}+C_oR$$

$$c = \frac{k_1(1-k_1)CC_pRR_c+CC_ok_1(1-k_1)RR_c+2k_1C_pC_oR_cR}{1+2C_p/C}.$$

Following the same analysis as in Section 2.2.3 but taking the parasitic capacitances C_p and C_o into account, the conditions for distortion cancellation at low frequencies are:

$$\frac{g_{m1}\cdot R\cdot(1-k_1)}{1+2C_p/C}=1 \quad , \quad k_2=\frac{k_1/2}{1+2C_p/C} \tag{2.7}$$

With the above provisions, the output current of the main OTA after algebraic simplifications is:

$$\begin{aligned} i_{out}(t) &= g_{m1}V_{i2}(t)+g_{m3}[V_{i2}(t)]^3 \\ &\approx g_{m1}V_{in}(t)\cdot\frac{(k_1/2)}{1+2C_p/C}\cdot\frac{1+j\omega C\left((1-k_1)R-k_1R_c\right)+j2\omega C_oR}{1+j\omega b-c\omega^2} \\ &- g_{m3}\left(\frac{k_1V_{in}(t)/2}{1+2C_p/C}\right)^3\cdot\frac{1+j\omega Ck_1R_c}{1+j\omega b-c\omega^2} \\ &+ g_{m3}\left(\frac{k_1V_{in}(t)/2}{1+2C_p/C}\cdot\frac{1+j\omega C\left((1-k_1)R-k_1R_c\right)+j2\omega C_oR}{1+j\omega b-c\omega^2}\right)^3 \end{aligned} \tag{2.8}$$

Assuming weakly non-linear operation based on condition iii) in Section 2.2.3 and that the signal can be expressed as a sum of sinusoids with noncommensurate frequencies, the harmonic input method can be applied to calculate the Volterra series coefficients [21] and theoretically demonstrate the non-linearity cancellation with the proposed scheme. Taking a single input $V_{in}(t)=e^{j\omega_1 t}$ and substituting into (2.8) to express the linear transfer function H_1:

$$H_1=g_{m1}\cdot\frac{(k_1/2)}{1+2C_p/C}\cdot\frac{1+j\omega C\left((1-k_1)R-k_1R_c\right)+2j\omega C_oR}{1+j\omega b-c\omega^2} \tag{2.9}$$

Selecting $V_{in}(t)=e^{j\omega_1 t}+e^{j\omega_2 t}+e^{j\omega_3 t}$ and making the appropriate substitutions for calculation of the third-order transfer function (H_3) yields the following equality after

expansion and omission of all terms that do not contain the $\exp(j\omega_1 t + j\omega_2 t + j\omega_3 t)$ factor relevant to H_3:

$$\begin{aligned} &H_3(\omega_1,\omega_2,\omega_3) = \\ &g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3\left(\frac{1+j\omega_1 C\left((1-k_1)R-k_1R_c\right)+2j\omega_1 C_o R}{1+j\omega_1 b-c\omega_1^2}\right) \\ &\cdot\left(\frac{1+j\omega_2 C\left((1-k_1)R-k_1R_c\right)+2j\omega_2 C_o R}{1+j\omega_2 b-c\omega_2^2}\right)\left(\frac{1+j\omega_3 C\left((1-k_1)R-k_1R_c\right)+2j\omega_3 C_o R}{1+j\omega_3 b-c\omega_3^2}\right) \\ &-g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3\frac{1+j(\omega_1+\omega_2+\omega_3)Ck_1R_c}{1+j(\omega_1+\omega_2+\omega_3)b-c(\omega_1+\omega_2+\omega_3)^2} \end{aligned} \tag{2.10}$$

The amplitude of the third harmonic distortion (HD3) current due to a sinusoidal input signal $V_{in}sin(\omega t)$ is given by

$$\begin{aligned} &i_{o3} = \frac{1}{4}V_{in}^3 H_3(\omega,\omega,\omega) = \\ &\frac{1}{4}g_{m3}\left(\frac{V_{in}\ k_1/2}{1+2C_p/C}\right)^3\left(\frac{1+j\omega C\left((1-k_1)R-k_1R_c\right)+2j\omega C_o R}{1+j\omega b-c\omega^2}\right)^3 \\ &-\frac{1}{4}g_{m3}\left(\frac{V_{in}\ k_1/2}{1+2C_p/C}\right)^3\frac{1+j3\omega Ck_1R_c}{1+j3\omega b-9c\omega^2} \end{aligned} \tag{2.11}$$

Elimination of HD3 requires that $i_{o3} = 0$, hence

$$\frac{1+j\omega C\left((1-k_1)R-k_1R_c\right)+2j\omega C_o R}{1+j\omega b-c\omega^2} = \sqrt[3]{\frac{1+j3\omega Ck_1R_c}{1+j3\omega b-9c\omega^2}} \tag{2.12}$$

The cubic root in (2.12) can be approximated with $\sqrt[3]{1+x} \approx 1+x/3$ for $x << 1$. Thus,

$$\begin{aligned} &\frac{1+j\omega C\left((1-k_1)R-k_1R_c\right)+2j\omega C_o R}{1+j\omega b-c\omega^2} \approx \frac{1+j\omega Ck_1R_c}{1+j\omega b-3c\omega^2} \\ &\Rightarrow R_c \approx \frac{(1-k_1)+2C_o/C}{2k_1}R \qquad \text{to cancel HD3} \end{aligned} \tag{2.13}$$

For a two-tone input signal of the form $V_{in1}sin(\omega_1 t)+V_{in2}sin(\omega_2 t)$, the IM3 current can be determined with Volterra series according to the following equation:

$$\begin{aligned} i_{IM3} &= \frac{3}{4}V_{in1}^2 V_{in2} H_3(\omega_1,\omega_1,-\omega_2) = \\ & g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3 \left(3V_{in1}^2 V_{in2}/4\right)\left(\frac{1+j\omega_1 C\left((1-k_1)R-k_1R_c\right)+2j\omega_1 C_o R}{1+j\omega_1 b-c\omega_1^2}\right)^2 \\ & \cdot\left(\frac{1-j\omega_2 C\left((1-k_1)R-k_1R_c\right)-2j\omega_2 C_o R}{1-j\omega_2 b-c\omega_2^2}\right) \\ & - g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3 \left(3V_{in1}^2 V_{in2}/4\right)\frac{1+j(2\omega_1-\omega_2)Ck_1R_c}{1+j(2\omega_1-\omega_2)b-c(2\omega_1-\omega_2)^2} \end{aligned} \tag{2.14}$$

Simplifying i_{IM3} for two intermodulation tones that are close together ($\omega_1 \approx \omega_2 \approx 2\omega_1 - \omega_2$) yields:

$$\begin{aligned} i_{IM3} &\approx \frac{3g_{m3}V_{in1}^2 V_{in2}}{4}\left(\frac{k_1/2}{1+2C_p/C}\right)^3 \left(\frac{1+j\omega_1 C\left((1-k_1)R-k_1R_c\right)+2j\omega_1 C_o R}{1+j\omega_1 b-c\omega_1^2}\right)^2 \\ & \cdot\left(\frac{1-j\omega_1 C\left((1-k_1)R-k_1R_c\right)-2j\omega_1 C_o R}{1-j\omega_1 b-c\omega_1^2}\right) \\ & - g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3 \left(3V_{in1}^2 V_{in2}/4\right)\frac{1+j\omega_1 Ck_1R_c}{1+j\omega_1 b-c\omega_1^2} \\ \Rightarrow R_c &\approx \frac{(1-k_1)+2C_o/C}{2k_1}R \qquad for \quad i_{IM3}\approx 0 \end{aligned} \tag{2.15}$$

In the discussed example case with k_1=2/3, the condition to cancel IM3 with the phase shifter block in Fig. 2.5 is R_c=(R/4)*(1+6C_o /C). To ensure high linearity with variations of parasitic capacitances, the programmable range of R_c is selected based on process corner simulations as described in Section 2.5.

2.4 Circuit-Level Considerations

2.4.1Fully-Differential OTA with Floating-Gate FETs

Fig. 2.8 displays the schematic of the OTAs implemented on the 0.13μm CMOS test chip with a 1.2V supply, and its common-mode feedback (CMFB) circuit.

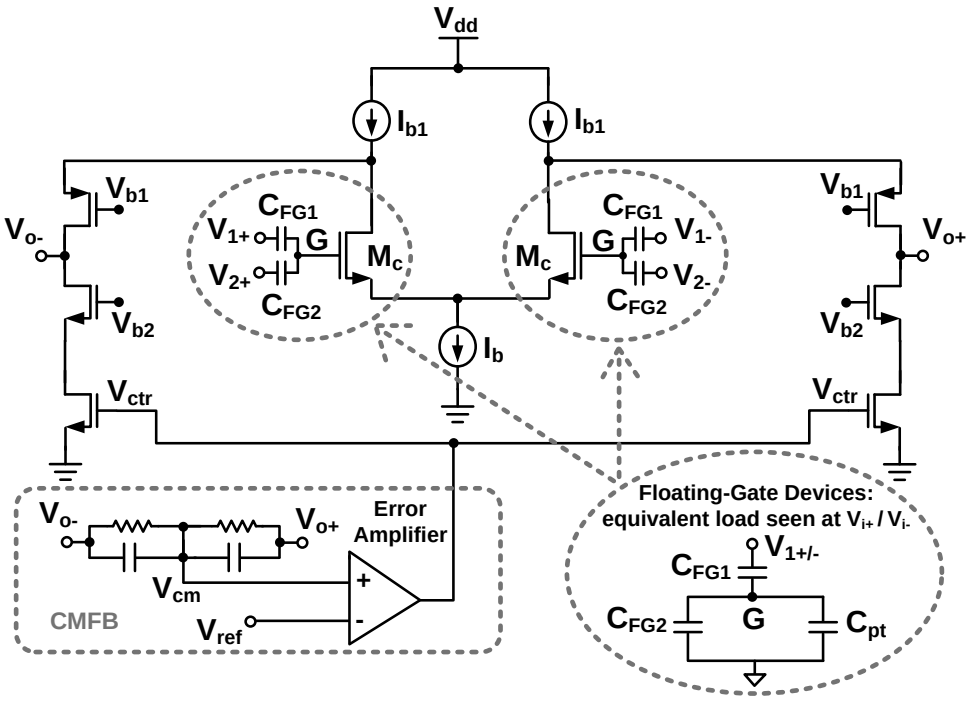


Fig. 2.8. Folded-cascode OTA (implements G_m in the main and auxiliary paths).

Attenuators k_1, $(1\text{-}k_1)$, and k_2 are realized with floating-gate devices for attenuation-predistortion linearization of this fully-differential topology. The gates (G) of the standard NMOS transistors in the OTA core are not resistively biased and are only connected to two conventional metal-insulator-metal (MIM) capacitors. Fig. 2.8 also

visualizes the equivalent capacitive load seen at the V_{1+} and V_{1-} inputs, where C_{pt} represents the effective gate-to-ground$_{(AC)}$ capacitance from transistor parasitic capacitances. With this configuration, the gate voltages are: $V_{G+/-} = (C_{FG1}/C_{total})V_{1+/-} + (C_{FG2}/C_{total})V_{2+/-}$, where $C_{total} \approx C_{FG1} + C_{FG2}$ when C_{pt} is negligible. It follows that the attenuation factors in Fig. 2.6 are: $C_{FG1}/C_{total} = k_1$ and $C_{FG2}/C_{total} = (C_{total}-C_{FG1})/C_{total} = 1-k_1$. The accuracy of the k_1 and $(1-k_1)$ factors predominantly depends on the matching of the MIM capacitors C_{FG1} and C_{FG2}, which can be achieved within 0.1-1% using proper layout techniques. As assessed in Section 2.5, such a matching accuracy is more than sufficient with the 3%-step programmability of resistor R for gain mismatch compensation in both paths.

In the layout, all nodes G at the floating gates in Fig. 2.8 are connected to the top metal layer using standard poly-metal contacts and metal-metal vias. During fabrication, this connection ensures that any charge stored on the floating gates flows to the substrate because all connections to the top metal are still joined prior to their separation during the last etching step. Thus, no charge is stored on the floating gates when the substrate contacts are also connected to the top metal layer [22], allowing gate discharge into the substrate before the last etching operation. After etching, the top metal extensions of the gates without trapped charge are floating, leaving only the connections to the two MIM capacitors. The floating-gate device design expressions for k_1 and $(1-k_1)$ above are assuming absence of excess charge on the floating gates, which is a satisfied condition without extra fabrication steps as a consequence of the gate and substrate connections to the top metal. A special programming technique for non-zero charge on the floating

gates was not utilized in this work, but a more sophisticated floating-gate device implementation as presented in [19] could be explored, which promises additional potential for compensation of inherent transistor threshold voltage offsets in the OTA's input differential pair.

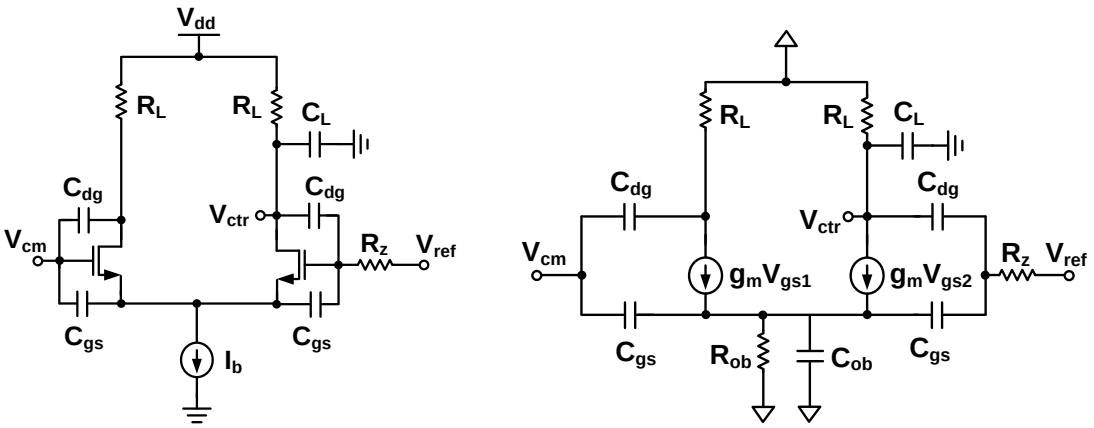
The phase shifter in Fig. 2.5 creates an extra pole within the linearized architecture that the reference OTA does not have. This phase delay is roughly the same as the delay from the pole formed by R and C_o in the auxiliary path. In low-loss (high-Q) designs, the additional pole can affect the gain of integrators and the frequency response of biquad sections if $1/(RC_o)$ is not significantly larger than the operating frequency. A load compensation scheme is discussed in Section 2.7 for such situations.

Identical standalone OTAs are included on the same die to obtain reference linearity measurements. The reference OTA also has a floating-gate input attenuation of 1/3 for fair performance comparison. In this way, the linearity benefit from the input attenuation is isolated from the architectural linearization proposed in Fig. 2.5, and both OTAs have the same effective transconductance (Gm/3 in this case), but the linearization results in doubled power consumption. Since attenuation and feedback linearization techniques have known linearity and effective transconductance trade-offs, the circuit-level comparison is focused on the predistortion linearization scheme relative to a commensurate OTA with equal input attenuation factor. This baseline OTA in Fig. 2.8 was biased with I_b = 0.95mA and I_{b1} = 0.85mA, having an effective transconductance of 510μA/V. The linearization does not require any design changes in this core OTA, but redesign of the OTA is an option if it is required to meet the same power budget after

linearization, which is possible as long as OTA bandwidth reduction can be tolerated. Such a linearization under power constraint is disclosed in Section 2.8.

2.4.2 Common-Mode Feedback Design

Suppression of undesired common-mode signals and noise is vital for linearity at high frequencies. The CMFB circuit should have high gain to accurately control the common-mode output voltage while maintaining a large bandwidth to reject common-mode noise in the band of interest. The CMFB amplifier is shown in Fig. 2.9, where V_{ctr} is the control voltage applied to the OTA in Fig. 2.8.



(a) (b)

Fig. 2.9. (a) Error amplifier circuit in the CMFB loop and (b) small-signal equivalent circuit.

Neglecting the effect of the output resistance R_{ob} and capacitance C_{ob} of the current source I_b in Fig. 2.9, the transfer function of the error amplifier is:

$$\frac{V_{ctr}}{V_{cm}} = \frac{g_m R_L}{2} \cdot \frac{1 + sR_z C_{dg} + s^2 R_z C_{dg} C_{gs} / g_m}{1 + 2s\zeta / \omega_n + s^2 / \omega_n^2} \tag{2.16}$$

where:

$$2\zeta / \omega_n = R_z (C_{dg} + C_{gs} / 2 + (g_m R_L / 2) C_{dg} + (R_L / R_z) \cdot (C_{dg} + C_L))$$

$$1 / \omega_n^2 = R_z R_L C_{dg} C_{gs} / 2 + R_z R_L (C_{dg} + C_{gs} / 2) C_L$$

The zeros of this transfer function are given by

$$\omega_{z1}, \omega_{z2} = -\frac{g_m}{2C_{gs}} \left(1 \pm \sqrt{1 - \frac{4C_{gs}}{g_m R_z C_{dg}}} \right) \tag{2.17}$$

and the pole locations in the transfer function are approximately:

$$\begin{aligned} \omega_{p1} &\approx -\frac{1}{R_z (C_{dg} + C_{gs} / 2 + (g_m R_L / 2) C_{dg} + (R_L / R_z) \cdot (C_{dg} + C_L))} \\ \omega_{p2} &\approx -\frac{C_{dg} + C_{gs} / 2 + (g_m R_L / 2) C_{dg} + (R_L / R_z) \cdot (C_{dg} + C_L)}{R_L C_{dg} C_{gs} / 2 + R_L (C_{dg} + C_{gs} / 2) C_L} \end{aligned} \tag{2.18}$$

The pole ω_{p1} is inversely proportional to the compensation resistor R_z. Another pole in the CMFB loop is formed at the output of the OTA: $\omega_{p3} \approx 1/(r_o C_o)^{-1}$, where r_o is the output resistance of the OTA and C_o is the load capacitance. Assuming that the CMFB gain-bandwidth (GBW) is larger than the two dominant poles ω_{p1} and ω_{p3}, the CMFB gain-bandwidth product can approximated as

$$GBW \approx \sqrt{A_0 \cdot \omega_{p1} \cdot \omega_{p3}} \approx \sqrt{A_0 \cdot \omega_{p3} \cdot \frac{2}{R_z (C_{gs} / 2 + (g_m R_L / 2) C_{dg})}} \tag{2.19}$$

where A_0 is the CMFB loop gain. The effect of the two zeros on the GBW was assumed to be negligible for simplicity; however their effect on the PM cannot be neglected and should be taken into account. A small R_z is desired to achieve high CMFB bandwidth.

However, the two zeros (ω_{z1}, ω_{z2}) tend to go to infinity as R_z approaches zero, which will have an adverse effect on phase margin. If $4C_{gs}/g_m R_z C_{dg} << 1$, the two zeros can be approximated as

$$\omega_{z1} \approx -\frac{1}{R_z C_{dg}} \quad , \quad \omega_{z2} \approx -\frac{g_m}{C_{gs}}\left(1-\frac{C_{gs}}{g_m R_z C_{dg}}\right) \tag{2.20}$$

Hence, the phase margin can be estimated as follows:

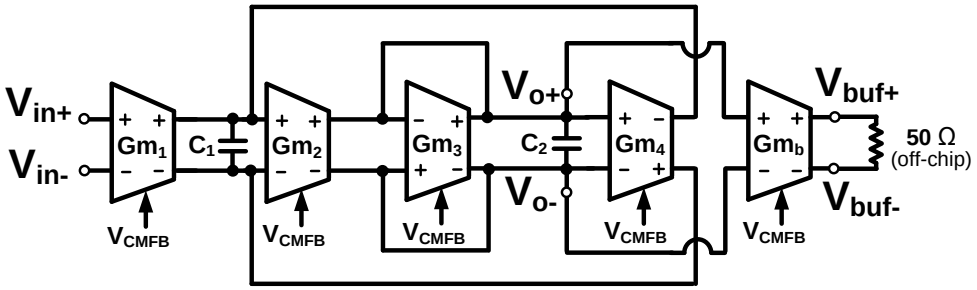
$$PM \approx \tan^{-1}\left(\sqrt{A_0 \cdot \omega_{p3} \cdot \frac{2R_z C_{dg}^2}{\left(C_{gs}/2+\left(g_m R_L/2\right)C_{dg}\right)}}\right) \tag{2.21}$$

Thus, the addition of the compensation resistor R_z results in two zeros in the transfer function of the error amplifier, which helps to insure stability of the CMFB loop. The simulated AC response of the CMFB loop has a 51.9dB low-frequency gain and a 424.9MHz unity-gain frequency with 42.5° phase margin.

2.4.3 Proof-of-Concept Filter Realization

A 2nd-order G_m-C biquad filter was designed with attenuation-predistortion-linearized OTAs to verify that the proposed methodology is suitable for filters with G_m-C integrator loops. Fig. 2.10 shows the filter schematic and specifications. The lowpass output of the biquad was measured using another OTA as buffer to drive the 50Ω input impedance of the spectrum analyzer.

The primary motivation for digital correction (Section 2.5) to enhance linearity performance with severe process variation is compatibility with digitally-controlled receiver calibration approaches that involve the baseband filter.



$$f_0 = \frac{1}{2\pi}\sqrt{\frac{G_{m2}G_{m4}}{C_1C_2}} \qquad Q = \frac{C_2}{G_{m3}}\sqrt{\frac{G_{m2}G_{m4}}{C_1C_2}}$$

Parameter	Value
Corner frequency (f_{3db})	194.7 MHz
Passband gain	0 dB
Output buffer gain (Gm_b x 50 Ω) & off-chip losses	-34.2 dB
$Gm_{1,2,3,4}$	510 µA/V

Fig. 2.10. Fully-differential 2nd -order lowpass filter diagram and design parameters.

Practical implementation details for receivers with digital performance monitoring and calibration of analog blocks are described in [23]-[25]. They incorporate accurate digital monitoring and I/Q mismatch correction in the digital signal processor (DSP) as well as a few analog observables that give some insights into the operating conditions, such as outputs from received signal strength indicators or DC control voltages of blocks. The possibility exists to generate and apply test tones at the input of an analog block and extract performance indicators from the output spectrum in the DSP, which contains distortion components. Conversely, calibration could also be performed by monitoring the bit error rate (BER) in the DSP from processing a special test sequence or customary pilot symbols at the beginning of receptions. Since linearity degradation impacts the BER, such a calibration could be computationally more efficient

than calculating and analyzing the fast Fourier transform in the DSP. Regardless of the specific digital calibration algorithm, the digitally-controlled correction capability of the proposed linearization scheme can potentially enable filter linearity tuning in integrated receiver applications without the need for extra DACs.

An alternative automatic calibration that does not involve an on-chip DSP but dedicated analog and simpler digital logic circuitry is displayed in Fig. 2.11.

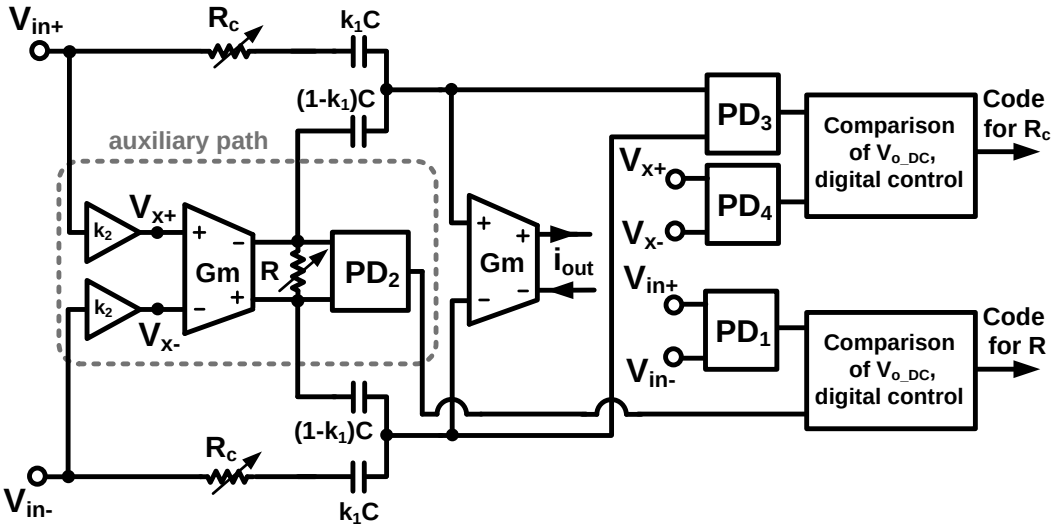


Fig. 2.11. Block diagram of the proposed automatic linearity tuning scheme.

From the conditions for optimum distortion cancellation described in Section 2.2.3, the gain of the auxiliary path must be equal to k_2G_mR, which is unity in the discussed design example. This can be ensured by measuring the signal level at the input and output of the auxiliary OTA with power or peak detectors (PD_1, PD_2), and controlling the digital code of resistor R until the gain is unity. The simplest control

algorithm would be to cycle through the codes that determine the value of R until the difference in the DC output voltages of PD_1 and PD_2 is minimized, which can be performed digitally by detecting the toggling instance at the output of a single comparator. At higher frequencies, the parasitic pole in the auxiliary path starts to affect the distortion cancellation, causing the signal level at the output of the auxiliary OTA to decrease with increasing frequency. Hence, the differential input signal to the main OTA at PD_3 increases as a result, which is shown in Fig. 2.12.

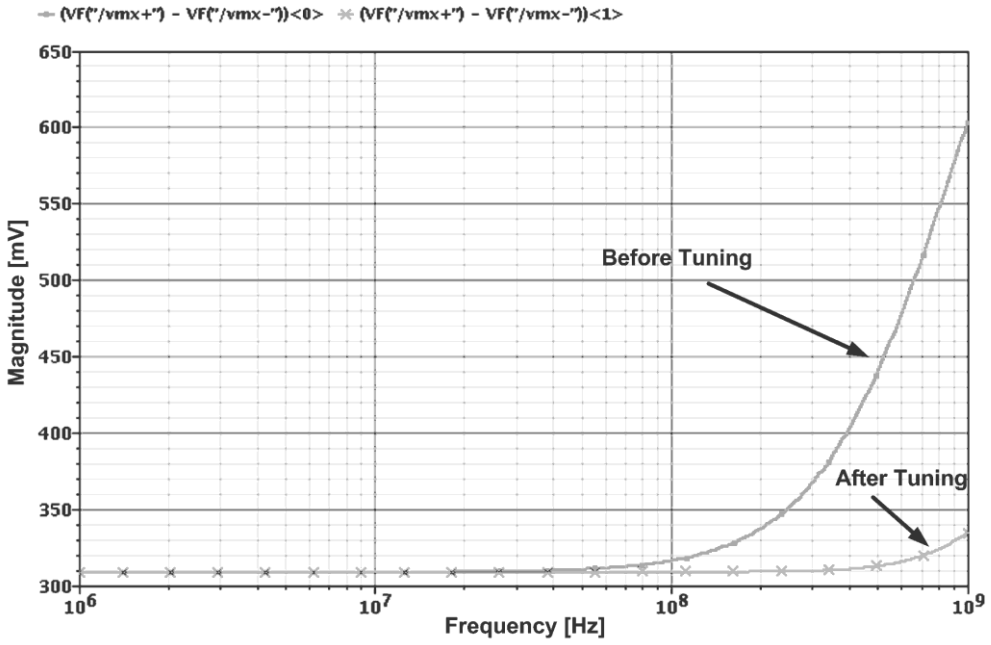


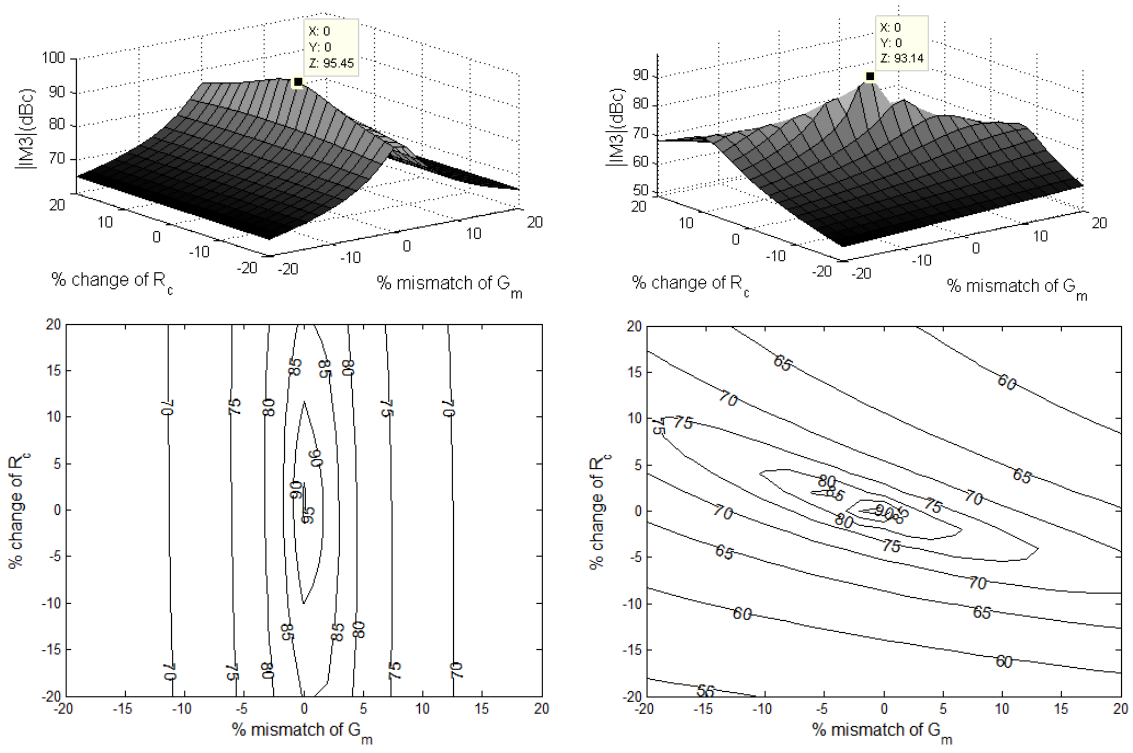
Fig. 2.12. Simulated AC amplitude at the input of the main OTA (PD_3 in Fig. 2.11) before and after adjustment of resistor R_c to its optimum value. (The voltage at PD_3 is ideally equal to $V_x = k_2 \cdot V_{in}$).

By measuring this signal that is ideally equal to $k_2 \cdot V_{in}$ with PD_3, the value of the phase shift resistor R_c can be adjusted until the outputs of PD_3 and PD_4 are equal. This comparison can be completed with the same logic as for PD_1/PD_2, but it has to be done with an input signal at the maximum frequency at which high linearity is desired. The automatic tuning has not been implemented on the circuit level, but simulations with different values of R_c showed that amplitude detection within 4.6% is required to detect R_c changes within 5% at 350MHz, which is sufficient for IM3 higher than 70dBc (Section 2.5). In differential gain measurements, PVT errors in the detectors are cancelled except for the errors from unavoidable mismatches between the two detectors. Errors from mismatches are less than 5% at 2.4GHz [26], and more accurate amplitude detection is achievable at lower frequencies. In [27] for example, differential on-chip amplitude measurements were conducted up to 2.4 GHz using detectors with a die area of $0.031mm^2$ and negligible loading of the signal path ($C_{in} < 15fF$).

2.5 Compensation for PVT Variations and Frequency-Effects

Since the frequency compensation is based on equalization of phase shifts from RC time constants in the main and auxiliary paths, the optimum linearity point is subjected to PVT variations. Resistors R and R_c in Fig. 2.5 can be adjusted digitally to ensure high linearity. When implementing the attenuation ratios with matched capacitors, the variation of the resistors and transconductance mismatch between the auxiliary and main paths become the main sources of IM3 degradation. Fig. 2.13

illustrates the technique's sensitivity to 20% variation of R_c and G_m based on expression for IM3 in (2.15).



(a) (b)

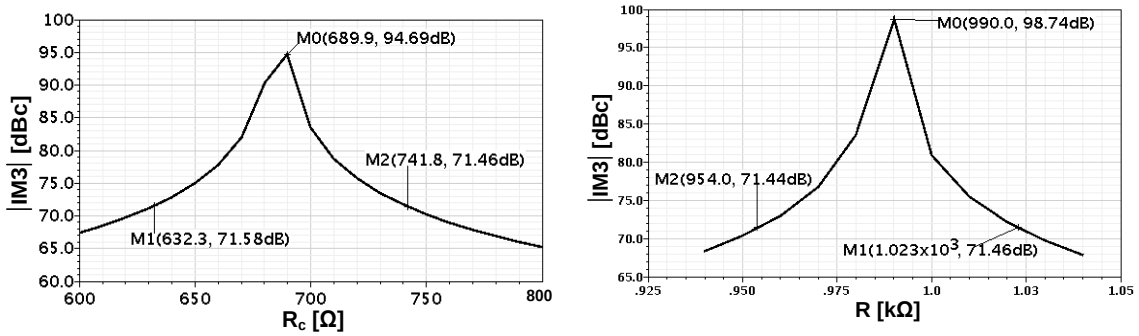
Fig. 2.13. Sensitivity of |IM3| (in dBc) to component mismatches calculated with equation (2.15): (a) 10MHz signal frequency, (b) 200MHz signal frequency.

In theory, the |IM3| (in dBc) without parameter variation is infinite. After introducing a numerical resolution constraint, the peak |IM3| is limited to around 95dBc. Fig. 2.13 (a) reveals that G_m-mismatch results in more degradation than R_c variation at low frequencies, but at high frequencies variation of R_c becomes equally significant as

evident from Fig. 2.13 (b). In general, less than ±10% mismatch of $G_m \times R$ and ±5% variation of R_c are required for theoretical |IM3| higher than 70dBc. Under consideration of the trend towards increasing intra-die variability in modern CMOS processes, programmability of R and R_c is necessary to guarantee $G_m \times R$ gain and R_c values within these limits. The determination of the appropriate incremental resistor step size is elaborated next.

To obtain a practical assessment of the distortion cancellation sensitivity, the compensation resistor value and transconductance mismatch in the two paths were varied in circuit simulations using Spectre. The resulting |IM3| is plotted vs. deviation from the nominal design parameters in Fig. 2.14, showing an |IM3| better than 71dBc for ±7.5% R_c-variation and |IM3| better than 71dBc for ±3.3% R-variation in the presence of 10% G_m-mismatch. The reference OTA has |IM3| of 51dBc. It is imperative for effective distortion cancellation to implement the resistor ladders with 3% steps, enabling digital correction of relatively small intra-die mismatches. To account for large absolute variations of parameters, the adequate resistor tuning range should be selected based on simulations under anticipated worst-case conditions.

In this work, simulations with process-corner models and temperatures ranging from -40°C to 100°C were conducted. Based on these simulation results, a conservative range from ~30 to 2.2kΩ (approximately 3% - 200% of the nominal value) and 6-bit resolution were chosen for the programmable resistors R_c and R (Fig. 2.5) in this prototype design.



(a) (b)

Fig. 2.14. Simulations showing sensitivity to variation and mismatch of critical components: (a) |IM3| vs. change in R_c (Fig. 2.5) at 350MHz, (b) |IM3| vs. R (in Fig. 2.5) with 10% transconductance mismatch between main OTA and auxiliary OTA at 350MHz.

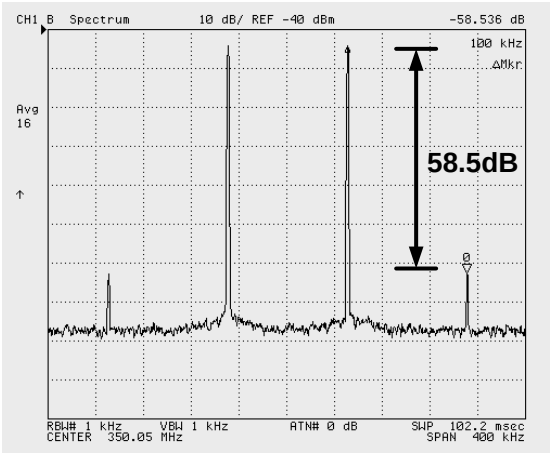
2.6 Measurement Results

2.6.1 OTA

Table 2.1 summarizes the characterization results for the OTA. Two $0.1V_{p\text{-}p}$ (-16dBm) tones with 100kHz frequency separation and a combined voltage swing of $0.2V_{p\text{-}p}$ were applied during IM3 measurements. The results in Fig. 2.15 demonstrate IM3 enhancement from –58.5dB to –74.2dB at 350MHz coupled with a rise in input-referred noise from 13.3nV/√Hz to 21.8nV/√Hz and twice the power dissipation, while other performance parameters are not affected significantly. The linearization decreased the SNR in 1MHz BW from 74.5dB to 70.2dB, but allowed to improve the IM3 by 15.7dB.

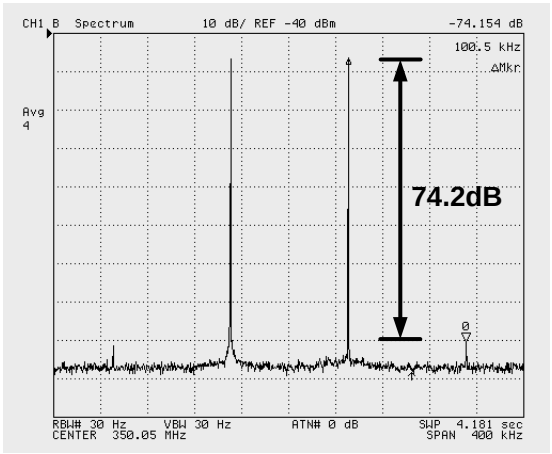
Table 2.1 Measured main parameters of the reference folded-cascode OTA.

Parameter	Measurement
Transconductance (G_m)	510 μA/V
IM3 @ 50MHz (Vin = 0.2 Vp-p)	-55.3 dB
Noise (input-referred)	13.3 nV/√Hz
Power with CMFB	2.6 mW
PSRR @ 50MHz	48.9 dB
Supply voltage	1.2 V



Uncompensated OTA IM3 (input: 0.2V_{p-p}@350MHz)

(a)



Compensated OTA IM3 (input: 0.2V_{p-p}@350MHz)

(b)

Fig. 2.15. Measured linearity with 0.2V_{p-p} input swing from two tones, each 0.1V_{p-p} (-16dBm) on-chip after accounting for off-chip losses at the input: (a) reference OTA, (b) compensated OTA.

Depending on the frequency and switch settings, IM3 enhancement up to 22dB was achieved with the compensation resistor ladders having 6-bit resolution. If more linearity improvement is required, the resolution of the resistor ladders (R and R_c) in Fig. 2.5 can be increased by adding more control bits or using a MOS in triode region as one of the elements to obtain a series resistance that is closer to the optimum value for distortion cancellation.

The IM3 from the two-tone tests of the reference and linearized OTAs around 350MHz is plotted versus input peak-to-peak voltage in Fig. 2.16. This comparison demonstrates that the IM3 enhancement from the linearization scheme requires weakly non-linear operation.

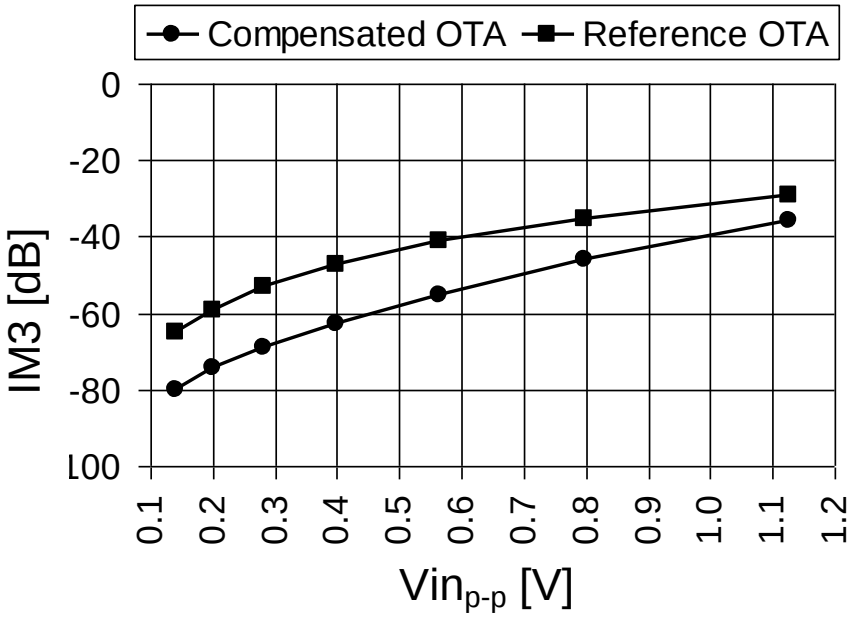


Fig. 2.16. Measured IM3 vs. input peak-peak voltage for reference OTA and compensated OTA obtained using two tones having 100kHz separation around 350MHz.

Even though the linearization effectiveness decreases with increasing input signal swing, the IM3 improvement is still 11dB with $0.8V_{p\text{-}p}$ differential signal swing for this design with 1.2V supply. Since the distortion cancellation exhibits the highest sensitivity to phase shifts at high frequencies, the control code of the phase shift resistor R_c in Fig. 2.5 has been changed from its optimum value. The resulting effect on the IM3 of the linearized OTA at 350MHz is plotted in Fig. 2.17, which validates that variable phase compensation is in fact required for optimum linearity performance. Two resistor ladder settings satisfy that the IM3 attenuation is more than 74dB, hence the selected 3% step for the least significant digital bit in this design was appropriate. Together with the plot obtained by sweeping resistor R_c in simulations (Fig. 2.14a), the measurements indicate that the amount of IM3 improvement predominantly depends on the step size of the programmable resistor ladder, which promises even better distortion cancellation with finer resolution.

Table 2.2 includes noise and IM3 measurement results at various frequencies, demonstrating the effectiveness of the broadband linearization scheme with the associated input-referred noise. Performance trade-offs can be assessed with the figure of merit from [8]: FOM = NSNR + 10log(f/1MHz) , where NSNR = $SNR_{(dB)}$ + 10log[($IM3_N$ / IM3)(BW / BW_N)(P_N / P_{dis})] from [9], the SNR is integrated over 1MHz BW, IM3 is normalized with $IM3_N$ = 1%, bandwidth is normalized with BW_N = 1Hz, and power consumption is normalized with P_N = 1mW.

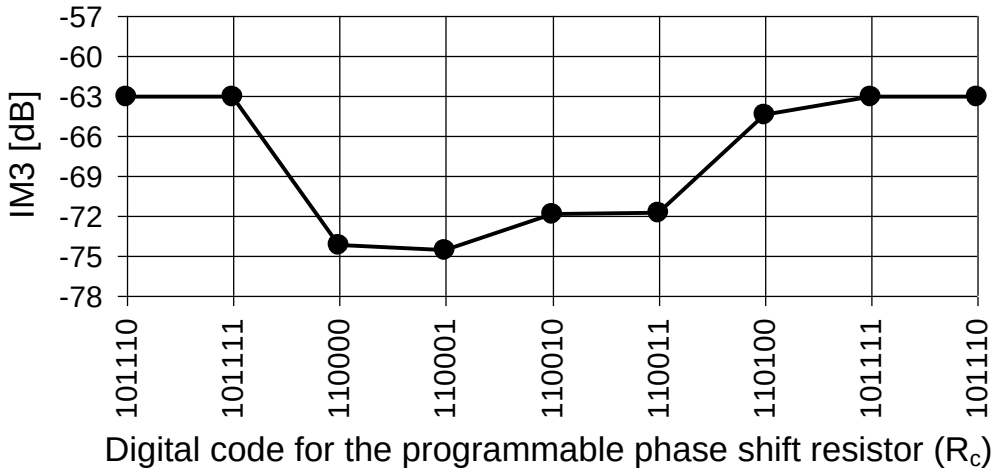


Fig. 2.17. Measured IM3 dependence of the compensated OTA on phase shift obtained with two test tones having 100kHz separation around 350MHz. (The least significant bit of the digital control code changes the value of phase shift resistor R_c by ~3%).

Table 2.2 Comparison of OTA linearity and noise measurements.

OTA type	Input-referred noise	Power consumption	IM3 (Vin = 0.2 V_{p-p})			Normalized |FOM|* (at 350 MHz)
			50 MHz	150 MHz	350 MHz	
Reference (input att. = 1/3)	**13.3 nV/√Hz**	**2.6 mW**	**-55.3 dB**	**-60.0 dB**	**-58.5 dB**	**56.7**
Linearized (att. = 1/3 & compensation)	**21.8 nV/√Hz**	**5.2 mW**	**-77.3 dB**	**-77.7 dB**	**-74.2 dB**	**64.3**

* See Table 2.3 for details.

Experimental results are compared with previously reported architectures in Table 2.3. The OTA linearized with input attenuation-predistortion shows a competitive performance with respect to the state of the art. High linearity at high frequencies is realized in this design example, showing the potential of the technique.

Table 2.3 OTA comparison with prior works.

	[1]*	**[11]***	**[14]**	**[12]**	**[7]***	**This work**
IM3	-	-47 dB	-70 dB	-60 dB	-	-74.2 dB
IIP3	-12.5 dBV	-	-	-	7 dBV	7.6 dBV
f	275 MHz	10 MHz	20 MHz	40 MHz	184 MHz	350 MHz
Input voltage	-	0.2 V_{p-p}	1.0 V_{p-p}	0.9 V_{p-p}	-	0.2 V_{p-p}
Power / transconductor	4.5 mW	1.0 mW	4 mW	9.5 mW	1.26 mW	5.2 mW
Input-referred noise	7.8 nV/√Hz	7.5 nV/√Hz	70.0 nV/√Hz	23.0 nV/√Hz	53.7 nV/√Hz	21.8 nV/√Hz
Supply voltage	1.2 V	1.8 V	3.3 V	1.5 V	1.8 V	1.2 V
Technology	65 nm CMOS	0.18 µm CMOS	0.5 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.13 µm CMOS
$FOM_{(dB)}$**	87.5	92.9	96.1	99.1	100	105.6
Normalized |FOM|***	1.0	3.4	7.1	14.3	17.8	64.3

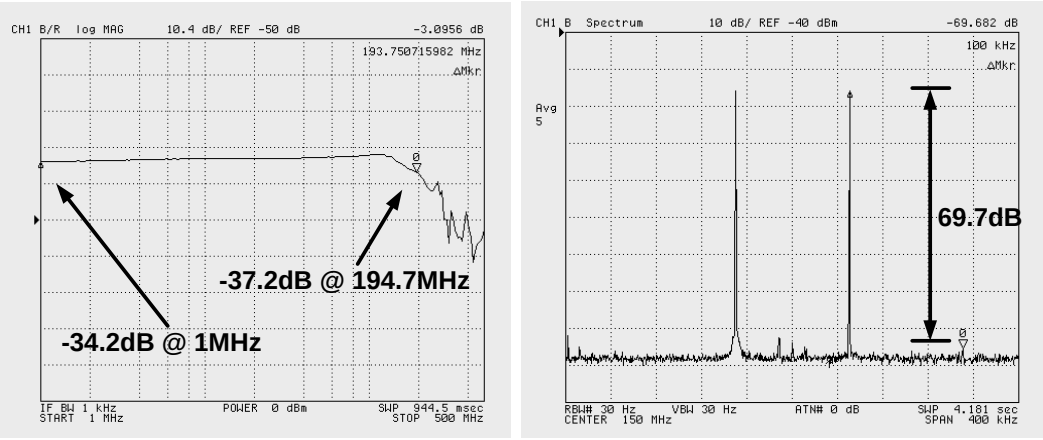
* Power/transconductor calculated from filter power. Individual OTA characterization results not reported in full.

** $FOM_{(dB)} = 10\log(f / 1MHz) + NSNR$ from [8] ; $NSNR = SNR_{(dB)} + 10\log[(IM3_N / IM3)(BW / BW_N)(P_N / P_{dis})]$ from [9].
(SNR integrated over 1MHz BW, normalization: $IM3_N = 1\%$, $BW_N = 1Hz$, $P_N = 1mW$)
(IM3 in FOM for [1] and [7] was calculated with: $IM3_{(dB)} = 2 \times [Pin_{(dBm)} - IIP3_{(dB)}]$.)

*** Normalized FOM magnitude relative to [1]: Normalized |FOM| = 10^($FOM_{(dB)}$/10) / (10^($FOM_{(dB)}$/10) of [1])

2.6.2 Second Order Low Pass Filter

Fig. 2.18 shows the filter frequency response for the proof-of-concept biquad design in Fig. 2.10, and its linearity performance is plotted against frequency in Fig. 2.19.



Frequency response of 2nd - order LPF

IM3 of the LPF with compensated OTAs (input: 0.2V_{p-p}@150MHz)

(a) (b)

Fig. 2.18. Filter measurements: (a) transfer function with ~34dB total losses (input loss and output buffer attenuation). (b) IM3 with 0.2V_{p-p} input swing from two tones, each 0.1V_{p-p} (-16dBm) on-chip after accounting for off-chip input losses.

The IM3 of the filter is up to 8dB worse than that of the standalone OTA. However, the measured filter IM3 includes approximately 2-3dB degradation due to the non-linearity of the output buffer. By adjusting the resistor ladders with digital controls that are common for all OTAs, the filter achieves IM3 ≈ -70dB up to 150MHz for a

$0.2V_{p-p}$ two-tone input. At 200MHz, the IM3 is -66.1dB, demonstrating the effectiveness of the broadband linearization due to compensation with the phase shifter.

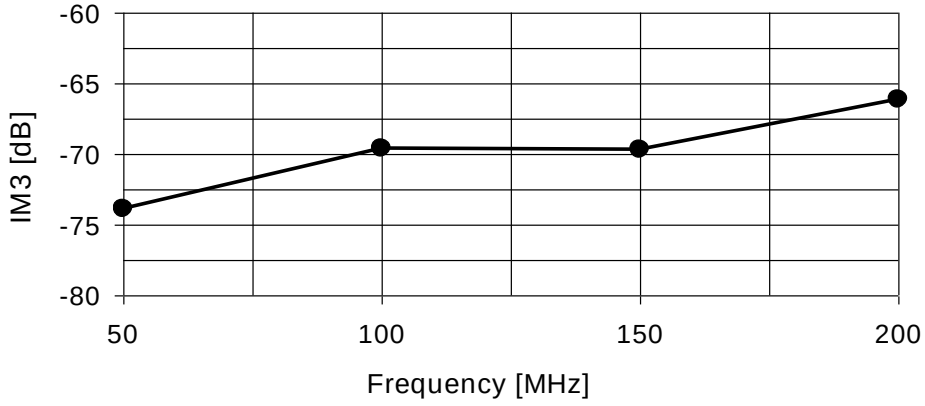


Fig. 2.19. Measured filter IM3 vs. frequency with two test tones having 100kHz separation.

Fig. 2.20 visualizes the measured IM3 with increasing input voltage up to 1.13V peak-peak differential swing, which follows the expected trend. At 150MHz, an IM3 of approximately -31dB occurs with an input signal of $0.75V_{p-p}$.

Fig. 2.21 illustrates the in-band IIP3 (14.0dBm) and IIP2 (33.7dBm) curves measured with two tones separated by 100kHz around 150MHz and 2MHz, respectively. In broadband receiver applications with limited filtering in the RF front-end, the presence of numerous out-of-band interference signals results in inter-modulation components within the desired signal band. Thus, high out-of-band linearity is desirable in addition to the baseband filter attenuation in order to minimize in-band distortion. This is one of the main motivations to employ OTAs with high linearity at high frequencies even for baseband filters with low cutoff frequencies.

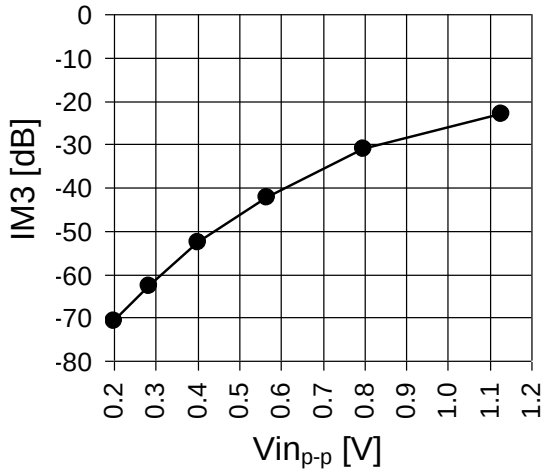
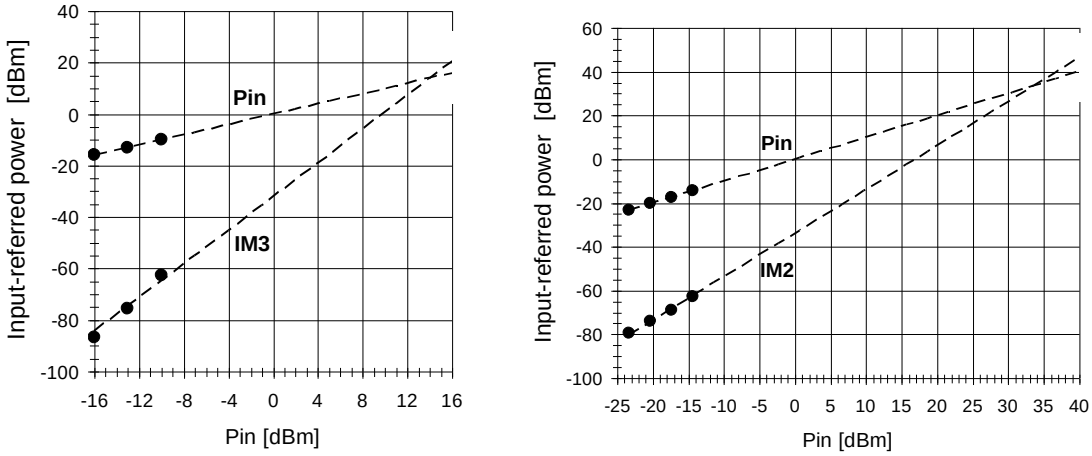


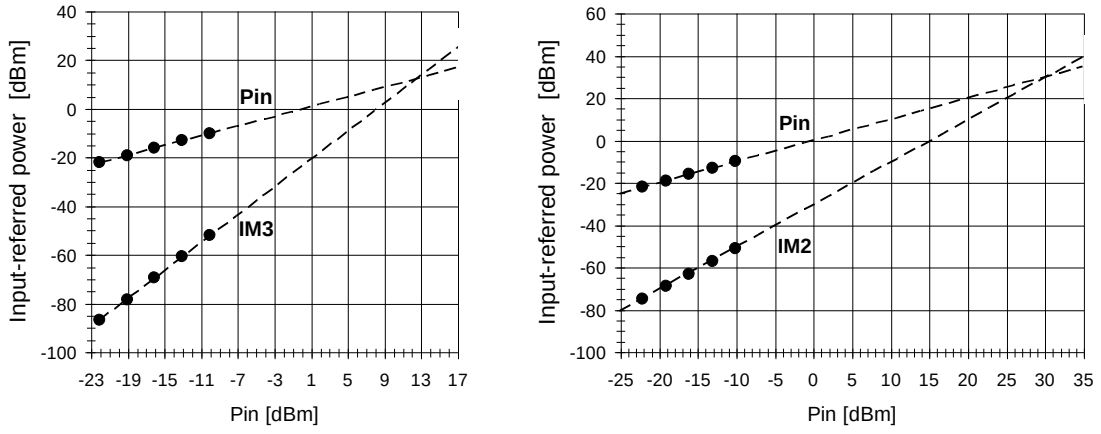
Fig. 2.20. Measured IM3 vs. input peak-peak voltage for the linearized filter obtained with two test tones having 100kHz separation around 150MHz.



(a) (b)

Fig. 2.21. Measured in-band intercept point curves for the filter: (a) IIP3 [two tones, Δf = 100kHz around 150MHz], (b) IIP2 [two tones, Δf = 100kHz around 2MHz].

The out-of-band IIP3 plot in Fig. 2.22a confirms that the linearization scheme's effectiveness is preserved beyond the cutoff frequency. The slight degradation of the out-of-band IIP3 to 12.4dBm is most likely due to the different phase shifts experienced by the 275MHz and 375MHz test tones from the input to node 2 in the auxiliary path (Fig. 2.5). The digital control code for the phase shift resistor R_c of the OTAs in the filter was set to optimize linearity in the 195MHz bandwidth, hence the linearity degradation due to the frequency difference of the out-of-band tones. The out-of-band IIP2 (Fig. 2.22b) is 30.4dBm, which is 3.3dB lower than the in-band IIP2 due to suboptimum phase shifts at 375MHz. Despite of that, the use of OTAs with high out-of-band linearity helps to reduce in-band distortion from out-of-band interferers in broadband scenarios. The filter area on the die (Fig. 2.23) is ~0.5mm^2 including the output buffer.



(a) (b)

Fig. 2.22. Measured out-of-band intercept point curves for the filter: (a) IIP3 [f_1 = 275MHz, f_2 = 375MHz, f_{IM3} = 100MHz], (b) IIP2 [f_1 = 375MHz, f_2 = 375.1MHz, f_{IM2} = 100kHz].

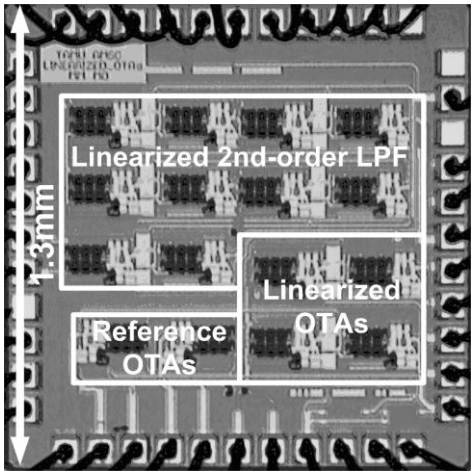


Fig. 2.23. Die micrograph of the OTAs and filter in 0.13µm CMOS technology. (Reference OTA area: 0.033mm^2, linearized OTA area: 0.090mm^2).

Table 2.4 summarizes its key performance parameters in contrast to other wideband lowpass filters. The 54.5dB dynamic range integrated over the 195MHz noise bandwidth is competitive with prior works having similar power consumption per pole, most of which were implemented under less voltage headroom constraints than with the 1.2V supply in this design. The proposed linearization is independent of OTA topology, but the proof-of-concept design is comprised of a restrictive fully-differential OTA core in order to demonstrate the concept with a conventional topology. The last two columns in Table 2.4 indicate that the proposed linearization allows almost similar filter linearity performance (in-band IIP3 = 14.0dBm with 1.2V supply) by means of fully-differential OTAs as with the pseudo-differential OTAs in [32], in which an in-band IIP3 of 16.9dBm was recently achieved with 1.8V supply. Apart from linearity considerations, the optimizations involving power consumption, input-referred noise, power supply noise rejection, and CMRR depend on the application-specific constraints. According to

the FOM comparison with the reference OTA in Table 2.2, the proposed linearization methods improves OTA linearity with favorable power and noise trade-offs. Furthermore, the most significant dynamic range improvement with the proposed technique can be achieved in bandpass designs, in which the noise is integrated over a narrow passband and the linearity improvement significantly reduces the power of the in-band distortion.

Table 2.4 Comparison of wideband G_m-C lowpass filters.

	[1]	[7]	[28]	[29]	[30]	[31]	[32]	This work
Filter order	5	5	8	4	7	5	3	2
f_c (max.)	275 MHz	184 MHz	120 MHz	200 MHz	200 MHz	500 MHz	300 MHz	200 MHz
Signal swing	-	0.30 V_{p-p}	0.20 V_{p-p}	0.88 V_{p-p}	0.80 V_{p-p}	0.50 V_{p-p}	-	0.75 V_{p-p}
Linearity with max. Vin_{p-p}	-	HD3, HD5: < -45dB	THD: -50dB @ 120MHz	THD: -40dB @ 20MHz	THD: -42dB @ 200MHz	THD: < -40dB @ 70MHz	-	IM3: -31dB **** @ 150MHz
In-band IIP3	-12.5 dBV (0.5 dBm)	7dBV (20dBm)	-	-	-	-	3.9 dBV (16.9 dBm)	1.0 dBV (14.0 dBm)
In-band IIP2	-	-	-	-	-	-	19 dBV (32 dBm)	20.7 dBV (33.7 dBm)
Out-of-band IIP3	-8 dBV (5 dBm)	-	-	-	-	-	-	-0.6 dBV (12.4 dBm)
Out-of-band IIP2	15 dBV (28 dBm)	-	-	-	-	-	-	17.4 dBV (30.4 dBm)
Power	36 mW	12.6 mW	120 mW	48 mW	210 mW	100 mW	72 mW	20.8 mW
Power per pole	7.2 mW	2.5 mW	15 mW	12 mW	30 mW	20 mW	24 mW	10.4 mW
Input-referred noise	7.8 nV/√Hz	53.7 nV/√Hz**	-	-	-	-	5 nV/√Hz	35.4 nV/√Hz
Dynamic range	44 dB*	43.3 dB***	45 dB	58 dB	-	52 dB	-	54.5 dB***
Supply voltage	1.2 V	1.8 V	2.5 V	2 V	3 V	3.3 V	1.8 V	1.2 V
Technology	65 nm CMOS	0.18 µm CMOS	0.25 µm CMOS	0.35 µm CMOS	0.25 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	0.13 µm CMOS

* Reported spurious-free dynamic range. ** Calculated from 9.3µV_{RMS} in 30kHz BW. *** Calculated from max. V_{p-p}, f_c, and input-referred noise density. **** IM3 of -31dB measured close to f_c ensures THD < -40dB.

2.7 Excess Phase Compensation

Fig. 2.24 shows the block diagram of a bandpass (BP) biquad. The inset in the figure displays a model for an OTA in integrator configuration, where r_o represents the OTA output resistance, C_o represents the output capacitance, and $Gm(j\omega)$ represents the transconductance that changes with frequency due to internal parasitic poles. Linearization introduces an additional pole ω_c that could influence the filter response at high frequencies. This pole can be cancelled by adding resistor $R_s = 1/(\omega_c C)$ in series with the load capacitor [33] to counteract the impact of excess phase on the quality factor based on the expression given in [2].

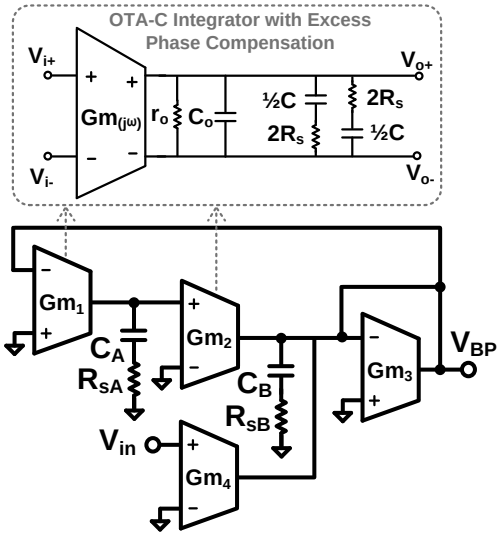
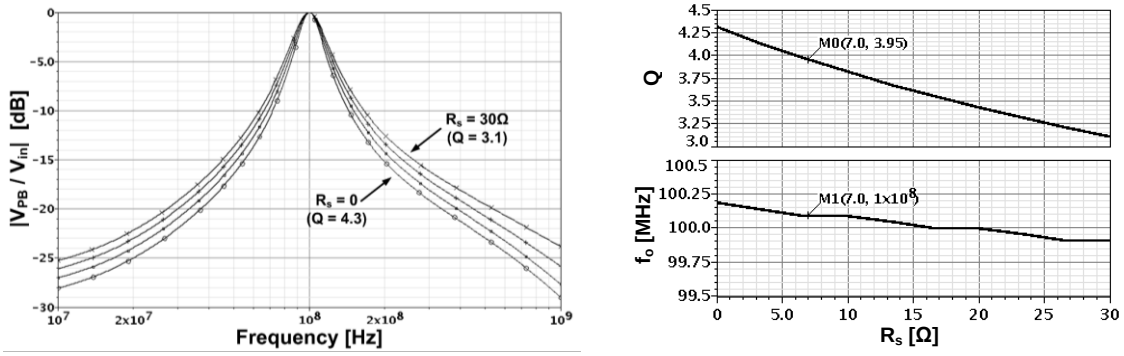


Fig. 2.24. Single-ended equivalent block diagram of a bandpass biquad.

The linearized OTAs described in Section 2.4.1 were employed in a BP filter (Fig. 2.24) with f_o = 100MHz, $Gm_3 = Gm_4 = Gm/2$, and $Gm = Gm_1 = Gm_2$ for simplicity

(implying $\omega_c = \omega_{c1} = \omega_{c2}$). Series resistors R_{sA} and R_{sB} with C_A and C_B compensate for the phase shift from the linearization by creating zeros ω_{zA} and ω_{zB}: $\omega_{zA} = 1/(R_{sA}C_A) = \omega_{zB} = 1/(R_{sB}C_B) = \omega_z = \omega_c$. A small BW error remains after compensation due to the difference between ω_z and ω_{c3} of Gm_3 because $\omega_{zA}(R_{sA}, C_A)$ and $\omega_{zB}(R_{sB}, C_B)$ are optimized to cancel ω_{c1} and ω_{c2} of Gm_1 and Gm_2, respectively. Thus, the pole ω_{c3} is only partially cancelled since $Gm_1 \neq Gm_3$. Nevertheless, the effect is small in the typical case ($\omega << \omega_{c3}$). This BP filter achieves simulated IM3 of -72.0dB evaluated after an additional output buffer (Gm). Fig. 2.25 contains simulated plots of the frequency responses for different values of R_s from this example BP filter design. The plots show how the adjustment of $R_s = R_{sA} = R_{sB}\cdot(C_B/C_A)$ during the design allows tuning of the quality factor to ~4 with $R_s = 7\Omega$ in this case, while f_o does not change significantly.



(a) (b)

Fig. 2.25. BP filter simulations with different R_s values for excess phase compensation: (a) frequency responses, (b) quality factor and center frequency; where $R_s = R_{sA} = R_{sB}\cdot(C_B/C_A)$.

2.8 Linearization without Power Budget Increase

Attenuation-predistortion linearization offers the means to improve the linearity of a given OTA while preserving its AC characteristics without design changes in the OTA core, which is achieved at the expense of increased power, noise, and layout area. Another option is to redesign the two OTAs in the linearization scheme using half of the power in order to meet the same power budget as the original OTA. But, that approach is associated with a reduction of the OTA bandwidth as delineated in this appendix.

To accomplish linearization with equal power budget, the currents I_b and I_{b1} in Fig. 2.8 can be reduced by 50%, which requires increasing the W/L ratios of the transistors in the core (M_c) to obtain the same transconductance as before. Thus, the saturation voltage V_{DSAT} of M_c becomes approximately half of the initial value. Furthermore, the ratio of transconductance to parasitic capacitance (i.e. f_T) of both OTAs in the linearization scheme reduces due to the bias current decrease and width increase for M_c. Gain vs. frequency simulations of the linearized OTA (50% power reduction in each path) and the reference OTA revealed that the linearization with equal power reduces the effective 3dB bandwidth from 2.49GHz to 1.09GHz with 50Ω load. Table 2.5 summarizes the key results from simulating the linearized OTA in comparison to the reference OTA with identical total power. High linearity through distortion cancelation (IM3 ≈ -77dB) is achievable, but limited to lower frequencies. Despite of this, the results indicate that higher FOM can be achieved with low-frequency linearization compared to the linearization with doubled power consumption.

Table 2.5 Simulated comparison: OTA linearization without power consumption increase.

OTA type	V_{DSAT} of input diff. pair (M_c)	f_{3db} with 50Ω load	Input-referred noise	Power	IM3 (V_{in} = 0.2 V_{p-p})	Normalized |FOM|* (at f_{max})
Reference (input att. = 1/3)	90 mV	2.49 GHz	9.7 nV/√Hz	2.6 mW	-53.1 dB at f_{max} = 350MHz (-53.2 dB at 100MHz)	57.2
Linearized (att. = 1/3 & compensation)	54 mV	1.09 GHz	14.3 nV/√Hz	2.6 mW	-77.1 dB at f_{max} = 100MHz	119.2

* See Table 2.3 for details.

CHAPTER III

HIGH EFFICIENCY CLASS D POWER AMPLIFIER FOR LOW POWER APPLICATIONS

3.1 Introduction

The demand of high performance wireless personal area network has led to the development of various standards such as Bluetooth [34] and UWB [35]. These standards enable the transmission of high data rate with adequate power consumption. Other applications such as sensor networks require low data rates and longer battery life. These requirements have led to the development of low power standards such as ZIGBEE [36] and MICS [37], where the data rate are below 1 Mbp and communication range is limited to about 2-10m with the transmitted power being less than 0 dBm.

Classical forms of implantable medical devices used magnetic coupling to communicate with external equipments. However, they require very close proximity of the reading device and they are prone to interferences from other radiating sources. Medical implant communication service (MICS) standard was developed to allow wireless connection between implantable medical chips and external equipment [38] for a distance of two meters or more [39]-[40]. To prolong the battery lifetime, MICS transceiver should be designed with the aim to minimize the power consumption. Since the sensitivity requirement of the implanted receiver is relaxed by the standard, the receiver power consumption can be minimized. On the other hand, the maximum allowed transmitter power of MICS standard should be limited to -2dBm [41]. To enable

the use of high efficiency transmitter, constant envelope modulation scheme is adopted by MICS system level designers. Constant envelope modulation allows the use of switching power amplifiers which exhibit high efficiency. Analysis and design of high efficiency power amplifier (PA) have been presented for high output power applications [42]-[44]. However, the growing demand on low output power transmitters make it necessary to develop new design techniques for high efficiency power amplifier. In this project the design and analysis of high efficiency power amplifiers for low output power applications will be presented and verified with experimental results.

3.2 High Efficiency Power Amplifier Architectures

The most common types of switching power amplifiers are class D PA and Class E PA. The main difference between class D and Class E is that the Class E PA uses harmonic shaping network to achieve zero voltage switching (ZVS) and thus it typically has higher efficiency than class D PA. In the following sections, an overview of both power amplifier classes are given with the advantages of each type in different applications.

3.2.1 Class E PA

Losses in switched mode power amplifier can be categorized into conduction losses due to finite switch resistance, and switching losses due to parasitic capacitor charging and discharging. To minimize conduction losses the switch on resistance should be minimized, however using large transistor to reduce the on resistance will

result larger parasitic capacitor and thus higher switching losses. Class E power amplifiers shown in Fig. 3.1 demonstrate high efficiency at high output power level since it uses soft switching and thus eliminates the switching losses [45]. The conditions to minimize the switching losses can be summarized as

1) Voltage reaches zero before the switch turns on.
2) Current flowing in the switch reaches zero before the switches turns off.
3) The slope of the voltage at turn on is zero, which will help to insure high efficiency operation even if the switching is shifted from its optimum point.

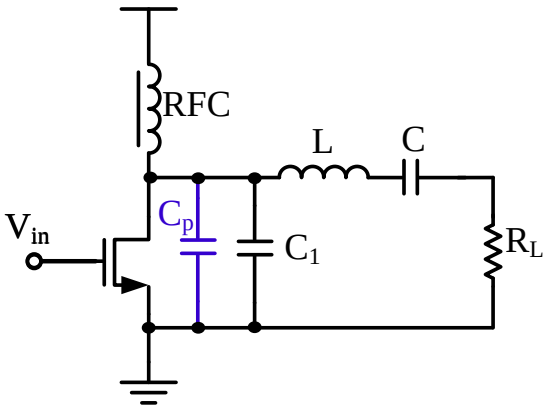


Fig. 3.1. Class E power amplifier.

Using these conditions, the value of the inductor, capacitors, and resistance are given by [45]

$$\begin{aligned} L &= Q_L R / 2\pi f \\ R_L &= \frac{8}{\left(\pi^2+4\right)} \frac{\left(V_{CC}-V_{ON}\right)^2}{P_{out}} \\ C_1 &= \frac{1}{2\pi f R}\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right) \\ C &\approx \frac{1}{\left(2\pi f\right)^2 L}\left(1+\frac{1.42}{Q_L-2.08}\right) \end{aligned} \quad , \tag{3.1}$$

where V_{ON} is the transistor on voltage, and Q_L is the quality factor of the output tank. The derivation of (3.1) is given in [46], in which it was assumed that Q_L is large enough such that the current flowing into output load resistance can be represented by the fundamental component only. Neglecting the transistor on voltage V_{ON}, the load resistance can be calculated from (3.1) to be 916Ω for a supply voltage of 1V and output power of -2 dBm. In this case the value of the inductance should satisfy the high Q_L condition, L >> R /2πf. For MICS standard, the frequency of operation is around 400 MHz, and the inductance at this frequency should be chosen such that L >> 364.5 nH. It is clear that the value of the inductor is too high and it will result very small value of the capacitor C. Hence, lower Q_L is desired in order to obtain more reasonable values of the circuit elements. Exact analysis for class E power amplifier with any value of Q_L is given in [47]. In general Q_L should not be too low in order to have low harmonic content at the output. For Q_L=1, the values of the circuit elements is given by [47]

$$\begin{aligned} R_L &= 0.4008\frac{V_{CC}^2}{P_{out}} \\ L &= 2.104R/2\pi f \\ C &= 2.104/2\pi fR \\ C_1 &= 0.2204/2\pi fR \end{aligned} \quad , \tag{3.2}$$

At 400 MHz, the circuit element values are R_L=636Ω, L=532.4nH, C=1.31PF, and C1=0.138PF, for output power of -2dBm and supply voltage of 1V. Using these values, the efficiency of ideal Class E PA is greater than 90 %. However, the high inductance value requires the use of off-chip inductors and package parasitics should be included in the simulation. By adding a parasitic capacitor of 1 PF at the drain of the

transistor, the efficiency decreases to less than 20%. Even after adding a resonating inductor to cancel the effect of the parasitic capacitance, the efficiency increases to about 46%. To achieve higher efficiency, the parasitic capacitor should be eliminated at harmonic frequencies. Although class E power amplifier shows superior efficiency, it is very sensitive to parasitics and the components values are not practical at low output power levels.

3.2.2 Class D PA

In class D switching PA [48], the voltage at the drain of the transistors takes the shape of a square wave that is filtered using the output tank. Fig. 3.2 shows class D power amplifier schematic and the associated voltage and current waveforms are depicted in Fig. 3.3. The efficiency of class D power amplifier is ideally 100%, however due to finite on resistance of the switches and the switching losses associated with charging and discharging of parasitic capacitors, the efficiency is typically around 70-90% for class D operation. Assuming that the quality factor of the output filter is high enough, the output current can be assumed to have only the fundamental component and other harmonic components can be neglected. Since half of the load current flows into the NMOS switch, while the other half flows into PMOS switch, the losses associated with the finite transistor on resistance can be written as

$$P_{L1} = I_{op}^2 \left(R_N + R_P \right) / 4 , \tag{3.3}$$

where I_{op}, R_N, and R_P are the peak value of the output current and the on resistance of NMOS and PMOS respectively.

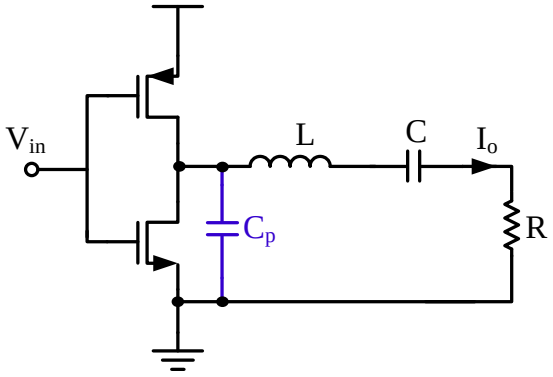


Fig. 3.2. Class D power amplifier.

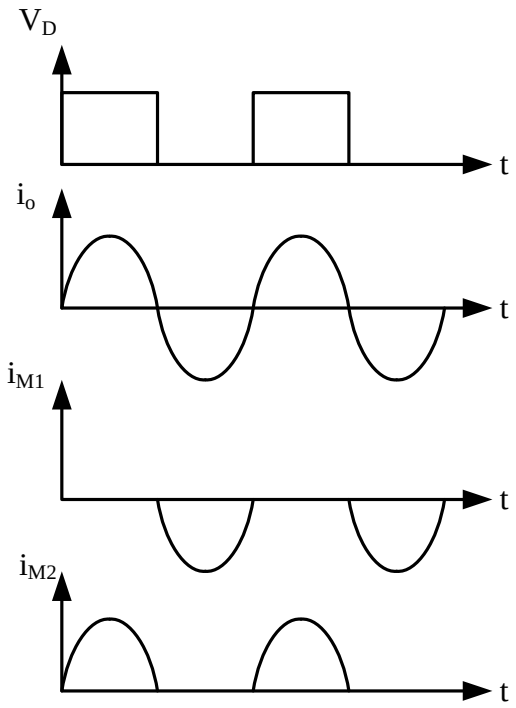


Fig. 3.3. Voltage and current waveforms of class D power amplifier.

The switching losses due to charging and discharging of C_p is given by

$$P_{L2} = V_{dd}^2 C_p f / 2, \tag{3.4}$$

where V_{dd} is the supply voltage and f is the operating frequency. Since the voltage at the drain of the transistors is a square wave with a peak value of V_{dd}, the fundamental component of this square wave is $2V_{dd}/\pi$. The peak value of the output current is given by

$$I_{op} = \frac{2V_{dd}}{\pi R_L} \tag{3.5}$$

Hence the efficiency of class D power amplifier is

$$\begin{aligned} \eta &= \frac{P_o}{P_o + P_{L1} + P_{L2}} = \frac{0.5I_{op}^2 R_L}{0.5I_{op}^2 R_L + 0.25I_{op}^2 (R_N + R_P) + (\pi R_L / 2)^2 I_{op}^2 C_p f / 2} \\ &= \frac{1}{1 + 0.5(R_N + R_P)/R_L + (\pi/2)^2 C_p f R_L} \end{aligned} \tag{3.6}$$

To enhance the efficiency, the on resistance of transistor should be minimized. Since the output power is $P_o = 2V_{dd}^2/\pi^2 R$, for low output power applications the value of the resistance should be high. Thus, the losses due to finite on resistance are lower for low output power since the ratio $(R_N+R_P)/R$ become smaller. However the impact of the switching losses increases as the output power becomes smaller. Techniques to improve the switching losses in class D power amplifier are discussed in the following section.

3.3 Zero Voltage Switching in Class D PA

The efficiency of class D power amplifier can be improved by using soft switching to reduce the switching losses [49]. The key idea is to switch off NMOS and PMOS devices at earlier time (Duty cycle <50%) to allow the output current to discharge the parasitic capacitance as depicted in Fig. 3.4. In soft switched class D PA, the charge

on the parasitic capacitance is turned into useful output current and thus the efficiency is improved. In [49] the input voltage is assumed to be a sine wave and the amplitude of the sine wave is selected to achieve the required delayed switch turn off.

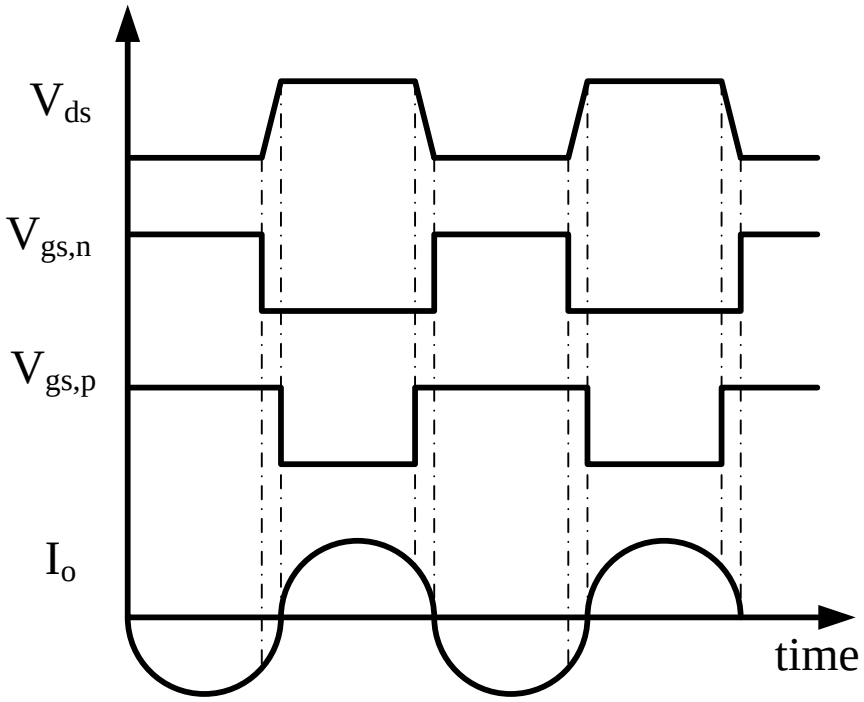


Fig. 3.4. Soft switching in class D power amplifier.

However, at low output levels the output current is very small near the switching point such that it will not be enough to discharge the parasitic capacitance. To solve this problem, the current at the switching point should be high enough to discharge the parasitic capacitance. Reducing the quality factor of the selective network will allow higher harmonics to flow and the current I_o will be closer to square waveform. The extra harmonics of the current I_o can be filtered using adding an extra parallel LC

tank added to the circuit, but this will increase cost of passive components needed. In the proposed solution, the matching network will be used as a filter of these extra harmonics since it is a step-up matching network.

For high power application, the load impedance should be small to get the desired output power. The value of the load resistance is $R_L = 2V_{dd}^2 / \pi^2 P_o$. Since the antenna impedance is typically chosen to be 50Ω, matching network should be used. For high power application the required R_L is typically less than 50Ω and step down matching network is used. On the other hand for low power application R_L is higher than 50Ω and a step up matching network is used. The step down matching network is shown in Fig. 3.5.

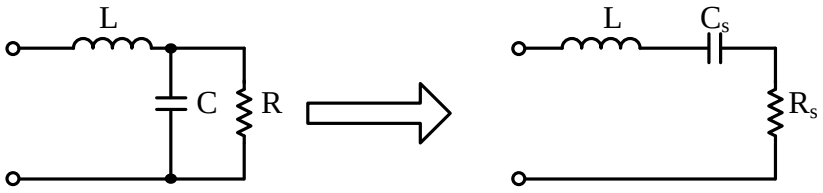


Fig. 3.5. Step down matching network.

The equivalent resistance R_s and capacitor C_s are given by

$$\begin{aligned} R_s &= R/\left(1+Q^2\right) \\ C_s &= \left(1+1/Q^2\right)C \end{aligned} \tag{3.7}$$

The inductance L in the step down matching network is used to resonate the capacitor and thus the input impedance equals R_s at the operating frequency. The step up matching network shown in Fig. 3.6 acts as a low pass filter and can be used to filter the

higher harmonics of the amplifier. The equivalent resistance R_p and inductance L_p of the matching network can be written as

$$\begin{aligned} R_p &= \left(1+Q^2\right)R \\ L_p &= \left(1+1/Q^2\right)L \end{aligned} \tag{3.8}$$

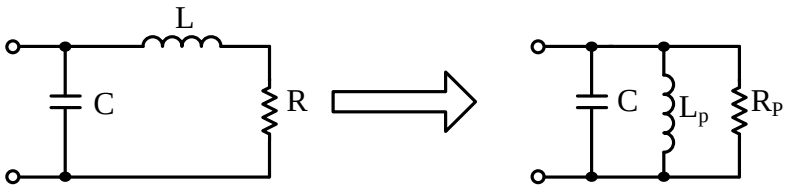


Fig. 3.6. Step up matching network.

The capacitor C is chosen to resonate with the inductance L_p at the frequency of operation, thus the input impedance of the matching network is purely resistive. Since the step up matching network acts as a low pass filter, the quality factor of the output tank can be reduced to allow more current harmonics as shown in Fig. 3.7. Very low Q will result square current waveform and thus the current at the switching edge will be high enough to achieve zero voltage switching. The square current waveforms will result in higher I_{rms} which in turn will increase the conduction losses in the MOS switches. The optimum current waveform is therefore somewhere in between the traditional sine wave and the square wave. In the following analysis, the first and the third order harmonics will be considered and optimized for the best efficiency.

The voltage at the drain of the transistors is a square wave with a finite fall and rise times. For simplicity, the rise and fall of the drain voltage is assumed to be of equal duration (ΔT) and a linear function of time, with the time origin chosen in the middle of the rising period.

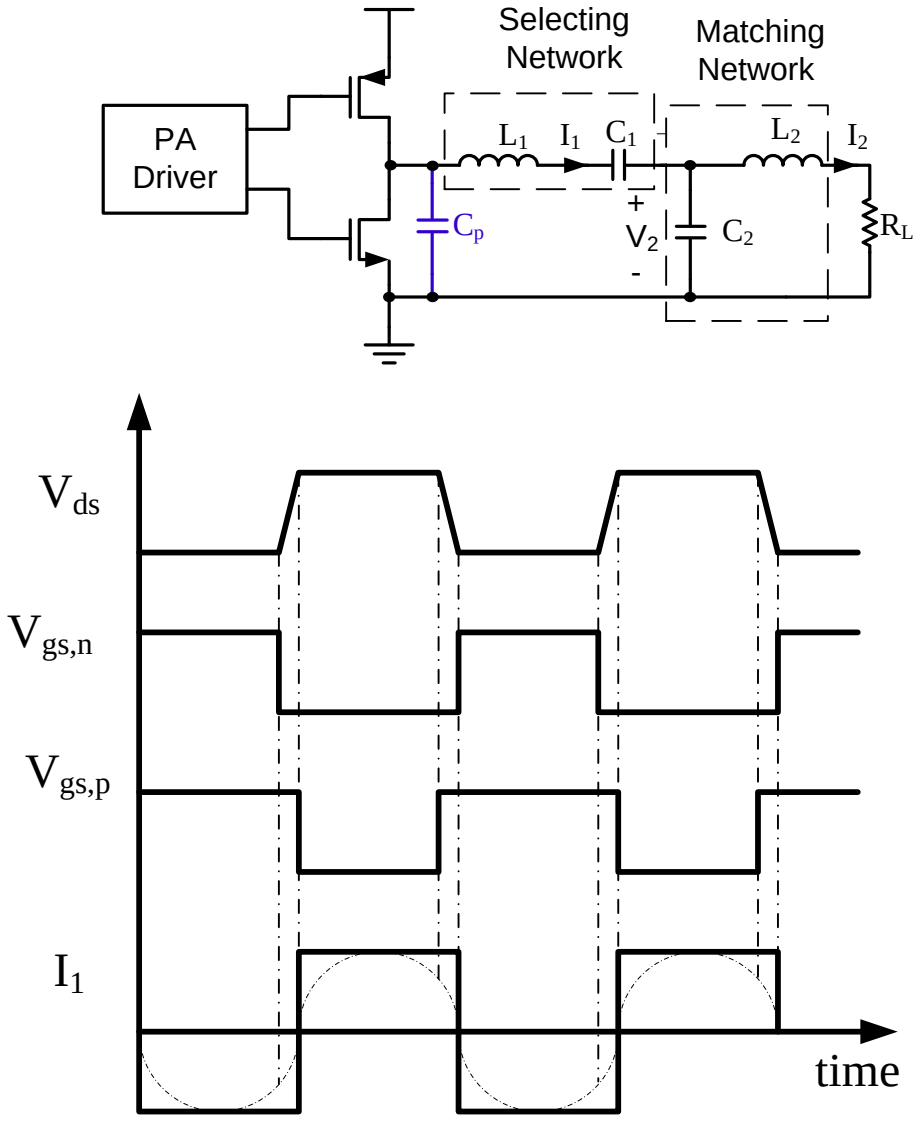


Fig. 3.7. Proposed current waveforms in soft switched class D power amplifier.

The drain voltage can be represented by Fourier series

$$
\begin{aligned}
&v(t) = a_0 + \sum_{n=1,3,..}^{\infty} a_n \sin(n\omega_0 t), \qquad \omega_0 = 2\pi / T \\
&a_0 = \frac{1}{T}\int_0^T v(t)dt = V_{dd}/2 \\
&a_n = \frac{8}{T}\int_0^{T/4} v(t)\sin(n\omega_0 t)dt = \frac{2V_{dd}}{n\pi}\operatorname{sinc}(n\omega_0 \Delta T/2) \\
&where\ \operatorname{sinc}(x) = \sin(x)/x
\end{aligned}
\tag{3.9}
$$

Taking into account the finite Q of the inductors, the admittance at the input of the matching network is given by

$$
\begin{aligned}
&Y_2 = SC_2 + \frac{1}{SL_2 + R_2}, \quad R_2 = R_L + r_{L2} \\
&Y_2 = j\omega C_2 + \frac{R_2 - j\omega L_2}{R_2^2 + (\omega L_2)^2}
\end{aligned}
\quad , \tag{3.10}
$$

where r_{L2} is the resistance in series with the inductor L_2 due to its finite quality factor. At the fundamental frequency, the input impedance of the matching network is purely resistive and it is given by 3.8. However at the harmonic frequencies, the impedance at the input of the matching network is

$$
\begin{aligned}
Z_2 &= \frac{SL_2 + R_2}{S^2 C_2 L_2 + SC_2 R_2 + 1} \\
Z_2\big|_{n\omega_0} &= \frac{jn\omega_0 L_2 + R_2}{-n^2\omega_0^2 C_2 L_2 + jn\omega_0 C_2 R_2 + 1} \\
&= \frac{R_2(1 + jnQ_2)}{-n^2/(1+1/Q_2^2) + jn(1+1/Q_2^2)/Q_2 + 1} \\
&\approx \frac{R_2(1+jnQ_2)(1+1/Q_2^2)}{jn(jnQ_2+1)/Q_2} = \frac{R_2(Q_2^2+1)}{jnQ_2} = \frac{R}{jnQ_2} \\
&where\ R = R_2(1+Q_2^2), C_2 = \frac{1}{(\omega_0^2 L_2)(1+1/Q_2^2)}
\end{aligned}
\tag{3.11}
$$

The capacitor C_1 resonate with the inductor L_1 at the operating frequency ($\omega_0 L_1 = 1/\omega_0 C_1$), hence the voltage at the capacitor C_2 at the harmonics of ω_0 is

$$\left.\frac{V_2}{V_{in}}\right|_{n\omega_0} = \frac{Z_2}{j(n-1/n)\omega_0 L_1 + r_{L1} + Z_2} \approx \frac{Z_2}{jn\omega_0 L_1 + \omega_0 L_1 / Q_{L1} + Z_1} = \frac{R/\ jnQ_2}{j(n\omega_0 L_1 - R/nQ_2) + \omega_0 L_1 / Q_{L1}}, \quad (3.12)$$

where r_{L1} is the resistance of the inductor L_1. The current through the L_1 is given by

$$i_1 = \frac{2V_{dd}\,\mathrm{sinc}(\omega_0 \Delta T/2)}{\pi} \cdot \frac{\sin(\omega_0 t)}{R + r_{L1}} + \sum_{n=3,5,..}^{\infty} \left(\frac{2V_{dd}}{n\pi}\right) \cdot \frac{\sin(n\omega_0 t)\mathrm{sinc}(n\omega_0 \Delta T/2)}{j(n\omega_0 L_1 - R/nQ_2) + \omega_0 L_1 / Q_{L1}} \quad (3.13)$$

The power loss in the resistor r_{L1} is then given by

$$P_{rL1} = \frac{2V_{dd}^2}{\pi^2} \frac{\mathrm{sinc}^2(\omega_0 \Delta T/2) r_{L1}}{(R + r_{L1})^2} + \sum_{n=3,5,..}^{\infty} \frac{2V_{dd}^2}{n^2\pi^2} \frac{\mathrm{sinc}^2(n\omega_0 \Delta T/2) r_{L1}}{(n\omega_0 L_1 - R/nQ_2)^2 + (\omega_0 L_1 / Q_{L1})^2} \quad (3.14)$$

The matching circuit acts as a low pass filter and thus the output current is mainly fundamental current at ω_0

$$i_{2,fund} = \frac{2V_{dd}}{\pi} \cdot \frac{R}{R + r_{L1}} \cdot \frac{\mathrm{sinc}(\omega_0 \Delta T/2)}{R_2(1 + jQ_2)} \approx \frac{2V_{dd}}{\pi} \cdot \frac{\mathrm{sinc}(\omega_0 \Delta T/2)}{R_2(1 + jQ_2)} \quad (3.15)$$

Hence the power loss in the resistor r_{L2} is given by

$$P_{rL2} = \frac{2V_{dd}^2}{\pi^2} \cdot \frac{\mathrm{sinc}^2(\omega_0 \Delta T/2) r_{L2}}{R_2^2(1 + Q_2^2)} \quad (3.16)$$

Each transistor rms current is half the rms current of the resistor r_1, and both transistors will be ON for only (T/2 –ΔT), thus the power loss due to finite transistor resistance is

$$
\begin{aligned}
P_N &= \frac{V_{dd}^2 \alpha_1 \operatorname{sinc}^2(\omega_0 \Delta T/2) r_N}{\pi^2 (R+r_1)^2} + \sum_{n=3,5,..}^{\infty} \frac{V_{dd}^2}{n^2\pi^2} \frac{\alpha_n \operatorname{sinc}^2(n\omega_0 \Delta T/2) r_N}{(n\omega_0 L_1 - R/nQ_2)^2 + (\omega_0 L_1/Q_{L1})^2} \\
P_P &= \frac{V_{dd}^2 \alpha_1 \operatorname{sinc}^2(\omega_0 \Delta T/2) r_P}{\pi^2 (R+r_1)^2} + \sum_{n=3,5,..}^{\infty} \frac{V_{dd}^2}{n^2\pi^2} \frac{\alpha_n \operatorname{sinc}^2(n\omega_0 \Delta T/2) r_P}{(n\omega_0 L_1 - R/nQ_2)^2 + (\omega_0 L_1/Q_{L1})^2} \\
P_{tr} &= P_N + P_P = \frac{V_{dd}^2 \alpha_1 \operatorname{sinc}^2(\omega_0 \Delta T/2) \cdot (r_N + r_p)}{\pi^2 (R+r_1)^2} \\
&\quad + \sum_{n=3,5,..}^{\infty} \frac{V_{dd}^2}{n^2\pi^2} \frac{\alpha_n \operatorname{sinc}^2(n\omega_0 \Delta T/2)(r_N + r_p)}{(n\omega_0 L_1 - R/nQ_2)^2 + (\omega_0 L_1/Q_{L1})^2}
\end{aligned}
\quad , \qquad (3.17)
$$

where P_N and P_P are the losses due to NMOS switch and PMOS switch respectively, and $\alpha_n = 1-2\Delta T/T+\sin(n\omega_0\Delta T)/n\pi$.

Using (3.13) and ignoring the harmonics higher than the third order, the current through the inductor L_1 can be approximated as

$$
\begin{aligned}
& i_{rL1} = I_1 \sin(\omega_0 t) - I_3 \cos(3\omega_0 t) \\
& I_1 = \frac{2V_{dd} \operatorname{sinc}(\omega_0 \Delta T/2)/\pi}{R + r_{L1}}, I_3 = \frac{2V_{dd} \operatorname{sinc}(3\omega_0 \Delta T/2)/3\pi}{\sqrt{(3\omega_0 L_1 - R/3Q_2)^2 + (\omega_0 L_1/Q_{L1})^2}}
\end{aligned}
\qquad (3.18)
$$

To achieve zero voltage switching, the charge on the parasitic cap should be converted to output current during a time of ΔT in which both transistors are off. Hence,

$$
Q = C \cdot V_{dd} = \int_{T/2-\Delta T/2}^{T/2+\Delta T/2} i_{r1} dt = \int_{T/2-\Delta T/2}^{T/2+\Delta T/2} I_1 \sin(\omega_0 t) - I_3 \cos(3\omega_0 t) dt = \frac{2I_3}{3\omega_0} \sin\left(3\omega_0 \frac{\Delta T}{2}\right) \qquad (3.19)
$$

The duration ΔT should be chosen to allow enough time to discharge parasitic capacitor, however higher values of ΔT will affect the operation of the amplifier. Choosing ΔT to be T/12 then

$$
\begin{aligned}
& \frac{2I_3}{3\omega_0} \sin(3\pi \Delta T/T) = C \cdot V_{dd} \\
& \Rightarrow X_{L1} = \frac{2 \operatorname{sinc}(3\omega_0 \Delta T/2) \sin(3\omega_0 \Delta T/2)}{27\pi^2 C f_s} + R/9Q_2
\end{aligned}
\qquad (3.20)
$$

As mentioned before higher values of the third harmonic current component result less switching losses, however it will lead to high conduction losses due to finite resistance of switches. Assuming the third harmonic current component is less than the value given in (3.20) it will not be enough to achieve full zero voltage switching, the remaining charge on the parasitic capacitor and the associated switching losses are

$$\begin{aligned} Q &= C \cdot V_{dd} - \frac{\sqrt{2} I_3}{3\omega_0} \\ \Rightarrow P_{sw} &= 0.5 Q V_{dd} f_s = 0.5 C V_{dd}^2 f_s - \frac{I_3}{3\omega_0} \sin\left(3\pi \frac{\Delta T}{T}\right) \\ &= 0.5 C V_{dd}^2 f_s - \left(\frac{V_{dd}^2}{9\pi^2}\right) \frac{\operatorname{sinc}(3\omega_0 \Delta T/2) \sin(3\omega_0 \Delta T/2)}{\sqrt{(3X_{L1} - R/3Q_2)^2 + (\omega_0 L_1 / Q_{L1})^2}} \end{aligned} \tag{3.21}$$

Hence the total loss in class D power amplifier is given by the summation of all power losses

$$\begin{aligned} P_{loss} &= \frac{2\operatorname{sinc}^2(\omega_0 \Delta T/2) V_{dd}^2}{\pi^2} \frac{X_{L1}/Q_{L1} + 0.5 \cdot \alpha_1 \cdot (r_N + r_P)}{(R + X_{L1}/Q_{L1})^2} \\ &+ \sum_{n=3,5,..}^{\infty} \frac{2\operatorname{sinc}^2(n\omega_0 \Delta T/2) V_{dd}^2}{n^2 \pi^2} \frac{X_{L1}/Q_{L1} + 0.5 \cdot \alpha_n \cdot (r_N + r_P)}{(nX_{L1} - R/nQ_2)^2 + (X_{L1}/Q_{L1})^2} \\ &+ \frac{2V_{dd}^2}{\pi^2} \cdot \frac{\operatorname{sinc}^2(\omega_0 \Delta T/2) r_{L2}}{R_2^2 (1 + Q_2^2)} \\ &+ 0.5 C V_{dd}^2 f_s - \left(\frac{V_{dd}^2}{9\pi^2}\right) \frac{\sin(3\omega_0 \Delta T/2) \operatorname{sinc}(3\omega_0 \Delta T/2)}{\sqrt{(3X_{L1} - R/3Q_2)^2 + (X_{L1}/Q_{L1})^2}} \end{aligned} \tag{3.22}$$

The inductor L_2 and capacitor C_2 are chosen to match the antenna impedance to the required impedance for certain output power. Since the inductor L_1 will determine the band pass filter bandwidth and harmonic contents, the inductance value should be chosen to get the minimum losses. The condition to minimize the power losses can be obtained by differentiating the power loss with respect to the inductance value

$$\begin{aligned}
&\frac{\partial P_{loss}}{\partial X_{L1}} \approx \frac{2\,\mathrm{sinc}^2(\omega_0 \Delta T/2) V_{dd}^2}{\pi^2} \frac{1/Q_{L1}}{R^2} \\
&+ \frac{2\,\mathrm{sinc}^2(3\omega_0 \Delta T/2) V_{dd}^2}{9\pi^2} \frac{1/Q_{L1}(3X_{L1} - R/3Q_2) - 6(X_{L1}/Q_{L1} + 0.5 \cdot \alpha_3 \cdot (r_N + r_P))}{(3X_{L1} - R/3Q_2)^3} \\
&+ \left(\frac{V_{dd}^2}{3\pi^2}\right) \frac{\sin(3\omega_0 \Delta T/2)\mathrm{sinc}(3\omega_0 \Delta T/2)}{(3X_{L1} - R/3Q_2)^2} \\
&\approx -\frac{2\,\mathrm{sinc}^2(3\omega_0 \Delta T/2) V_{dd}^2}{3\pi^2} \frac{\alpha_3 \cdot (r_N + r_P)}{(3X_{L1} - R/3Q_2)^3} \\
&+ \left(\frac{V_{dd}^2}{3\pi^2}\right) \frac{\sin(3\omega_0 \Delta T/2)\mathrm{sinc}(3\omega_0 \Delta T/2)}{(3X_{L1} - R/3Q_2)^2} \\
&\frac{\partial P_{loss}}{\partial X_{L1}} = 0 \Rightarrow X_{L1} = \frac{2\alpha_3 \cdot (r_N + r_P)}{9\pi \Delta T/T} + R/9Q_2
\end{aligned} \tag{3.23}$$

The size of the switches should be chosen large enough to decrease their on resistance, however large switch size will result higher input capacitance and the power consumption of the pre-driver will increase due to higher switching losses. Since the switch resistance is inversely proportional to the transistor width, while the switch capacitance is directly proportional to the width, the transistor size should be optimized to minimize the power losses. The transistor on resistance and input capacitance can be written as

$$\begin{aligned}
r_{on} &= K_r / W \\
C_{gs} &= K_C W \ ,
\end{aligned} \tag{3.24}$$

where K_r and K_c are supply and technology dependent constants. After adding the losses due to the input capacitance of the switches, the power losses take the form

$$
\begin{aligned}
P_{loss} &= \frac{2\,\mathrm{sinc}^2(\omega_0 \Delta T/2) V_{dd}^2}{\pi^2} \frac{X_{L1}/Q_{L1} + 0.5\cdot\alpha_1\cdot(K_{rn}/W_n + K_{rp}/W_p)}{\left(R + X_{L1}/Q_{L1}\right)^2} \\
&+ \sum_{n=3,5,..}^{\infty} \frac{2\,\mathrm{sinc}^2(n\omega_0 \Delta T/2) V_{dd}^2}{n^2\pi^2} \frac{X_{L1}/Q_{L1} + 0.5\cdot\alpha_n\cdot(K_{rn}/W_n + K_{rp}/W_p)}{(nX_{L1} - R/nQ_2)^2 + \left(X_{L1}/Q_{L1}\right)^2} \\
&+ \frac{2V_{dd}^2}{\pi^2}\cdot\frac{\mathrm{sinc}^2(\omega_0 \Delta T/2) r_{L2}}{R_2^2(1+Q_2^2)} \\
&+ 0.5CV_{dd}^2 f_s - \left(\frac{V_{dd}^2}{9\pi^2}\right)\frac{\sin(3\omega_0 \Delta T/2)\,\mathrm{sinc}(3\omega_0 \Delta T/2)}{\sqrt{\left(3X_{L1} - R/3Q_2\right)^2 + \left(X_{L1}/Q_{L1}\right)^2}} \\
&+ 0.5K_{cn}W_n\cdot V_{dd}^2 f_s + 0.5K_{cp}W_p\cdot V_{dd}^2 f_s
\end{aligned}
\tag{3.25}
$$

The optimum transistor size is obtained by differentiating the power losses with respect to W_n and W_p

$$
\begin{aligned}
\frac{\partial P_{loss}}{\partial W_n} = 0 \Rightarrow W_n^2 &\approx \frac{2}{\pi^2}\frac{K_{rn}}{K_{cn} f_s}\left[\frac{\alpha_1\,\mathrm{sinc}^2(\omega_0 \Delta T/2)}{R^2} + \frac{\alpha_3\,\mathrm{sinc}^2(3\omega_0 \Delta T/2)}{9(3X_{L1} - R/3Q_2)^2}\right] \\
\frac{\partial P_{loss}}{\partial W_p} = 0 \Rightarrow W_p^2 &\approx \frac{2}{\pi^2}\frac{K_{rp}}{K_{cp} f_s}\left[\frac{\alpha_1\,\mathrm{sinc}^2(\omega_0 \Delta T/2)}{R^2} + \frac{\alpha_3\,\mathrm{sinc}^2(3\omega_0 \Delta T/2)}{9(3X_{L1} - R/3Q_2)^2}\right]
\end{aligned}
\tag{3.26}
$$

Using (3.23), the optimum transistor width can be written as

$$
\begin{aligned}
W_n^2 &\approx \frac{2K_{rn}\alpha_1\,\mathrm{sinc}^2(\omega_0 \Delta T/2)/\pi^2 K_{cn} f_s R^2}{1 - K_{rn}\sin^2(3\omega_0 \Delta T/2)/18\pi^2\alpha_3 K_{cn} f_s\left(K_{rn} + \sqrt{(K_{rp}K_{cp})(K_{rn}/K_{cn})}\right)^2} \\
W_p^2 &\approx \frac{2K_{rp}\alpha_1\,\mathrm{sinc}^2(\omega_0 \Delta T/2)/\pi^2 K_{cp} f_s R^2}{1 - K_{rp}\sin^2(3\omega_0 \Delta T/2)/18\pi^2\alpha_3 K_{cp} f_s\left(K_{rp} + \sqrt{(K_{rn}K_{cn})(K_{rp}/K_{cp})}\right)^2}
\end{aligned}
\tag{3.27}
$$

3.4 Circuit Level Implementation

Class D switching power amplifier has been implemented for MICS standard at 400 MHz with output power of -2dBm as specified by the standard. The power amplifier and its driver that provides the appropriate control for both switch types are discussed next in the following sections.

3.4.1 Class D PA Circuit

The power amplifier is fabricated in CMOS 90nm technology. The technology parameters can be extracted from simulation and they are listed in Table 3.1.

Table 3.1 Transistor parameters.

Parameter	Value
K_{rn}	0.5×10^{-3} Ω·m
K_{cn}	4.1×10^{-9} F/m
K_{rp}	1.43×10^{-3} Ω·m
K_{cp}	3.8×10^{-9} F/m

Using the procedure outlined in section 3.3, the transistor sizes and passive component values are given in Table 3.2 for output power of -2dBm at 400 MHz. Simulations were done to obtain the optimum component values and they are also shown in Table 3.2

3.4.2 PA Driver Circuit

Power amplifier driver should convert the input sine wave to the square wave necessary to drive the switching amplifier. Power amplifier driver is implemented as a

series of inverters followed by delay control for the NMOS and PMOS switches as shown in Fig. 3.8.

Table 3.2 PA circuit component values.

Parameter	Calculation ($\Delta T = T/12$)	Calculation ($\Delta T = T/10$)	Simulation
L_1	17.6 nH	13.1 nH	24 nH
C_1	9 PF	12 PF	6.6 PF
L_2	45.7 nH	45.4 nH	42 nH
C_2	2.9 PF	2.9 PF	2.5 PF
W_n/L_n	36 / 0.08	47 / 0.08	36 / 0.08
W_p/L_p	63 / 0.08	82 / 0.08	60 / 0.08

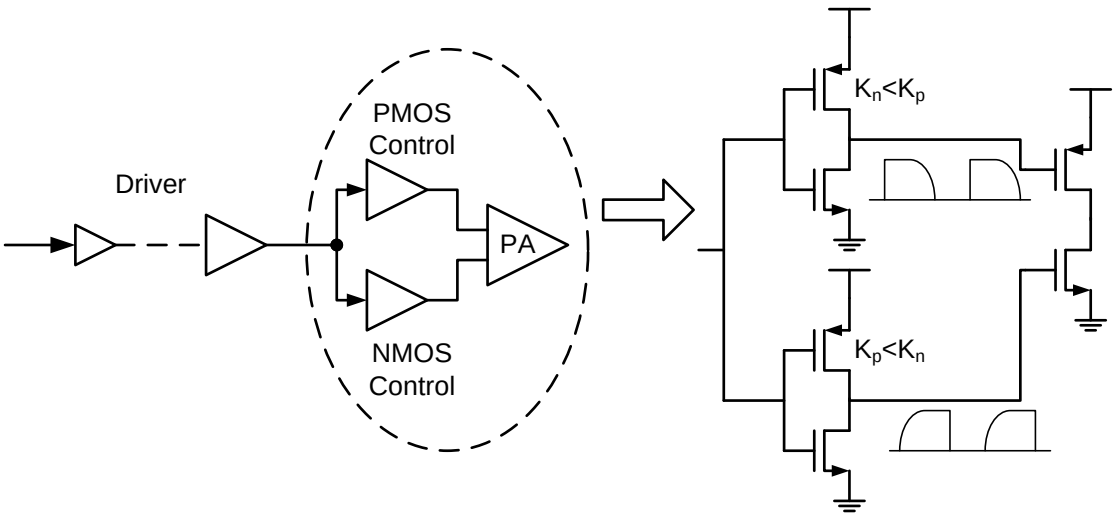


Fig. 3.8. Power amplifier driver circuit.

The PMOS switch has a CMOS driver which consists of a small NMOS transistor and a large PMOS transistor. When PMOS switch is off, its gate voltage is at V_{dd}. During the transient from off-state to on-state of PMOS switch, the small NMOS transistor in its driver slowly discharges the switch gate to the ground potential. On the other hand, NMOS switch driver has large NMOS transistor size and thus it will switch to the off-state before the PMOS switches to on-state such that there is enough time for the ZVS to take place. When NMOS is switched from off-state to on-state, the small PMOS transistor in its driver will slowly charge the switch gate and thus ZVS will be achieved.

3.5 Measurement Results

The power amplifier was fabricated in UMC 90 nm process; the power amplifier occupies 400μm^2 of chip area as shown in Fig. 3.9.

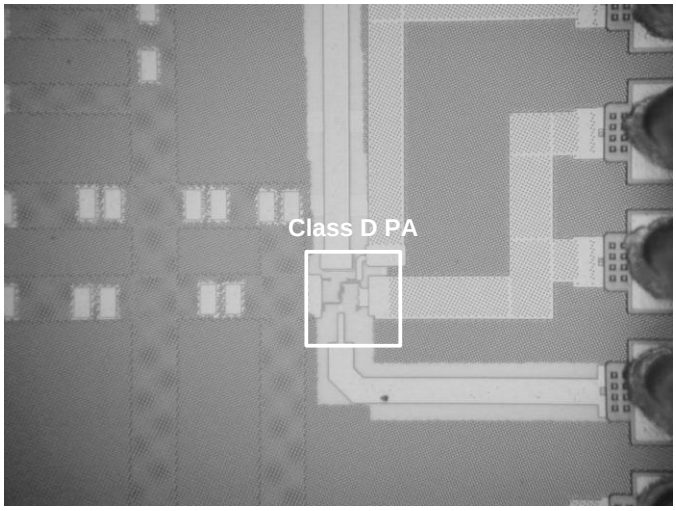


Fig. 3.9. Class D PA chip micrograph.

The output tank and matching networks are off-chip as shown in Fig. 3.10.

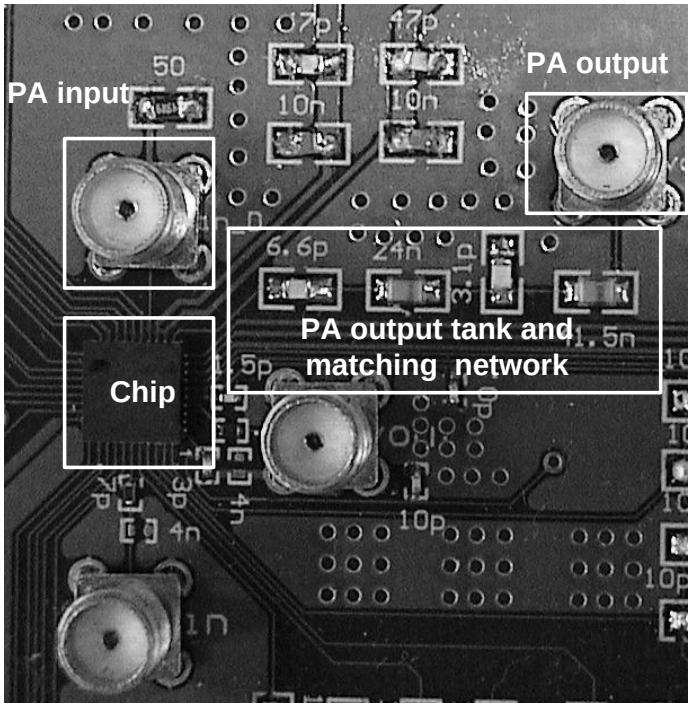


Fig. 3.10. PCB of class D power amplifier.

In order to absorb the trace inductance, its value has been taken into account when designing the matching network. The PCB trace connecting the passive components is much shorter than the wavelength at 400 MHz, hence it can be modeled using one inductor and two capacitors as shown in Fig. 3.11. For a standard FR-4 PCB with trace width of 6mil, the inductance per inch is approximately 20.9 nH and capacitance per inch is about 0.9 PF.

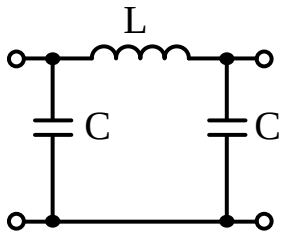


Fig. 3.11. PCB trace model.

The simulated and measured output power of the class D power amplifier are shown in Fig. 3.12 for different supply voltages. The corresponding power amplifier efficiency is displayed in Fig. 3.13.

Since the value of the parasitic capacitance at the output of the power amplifier might be larger than its estimated value of 1PF, the measured power efficiency is less than the values obtained from simulation. In addition, higher values of on resistance due to process variations, inaccuracies in the PCB trace parasitics values, or output passive component values also lead to lower efficiency.

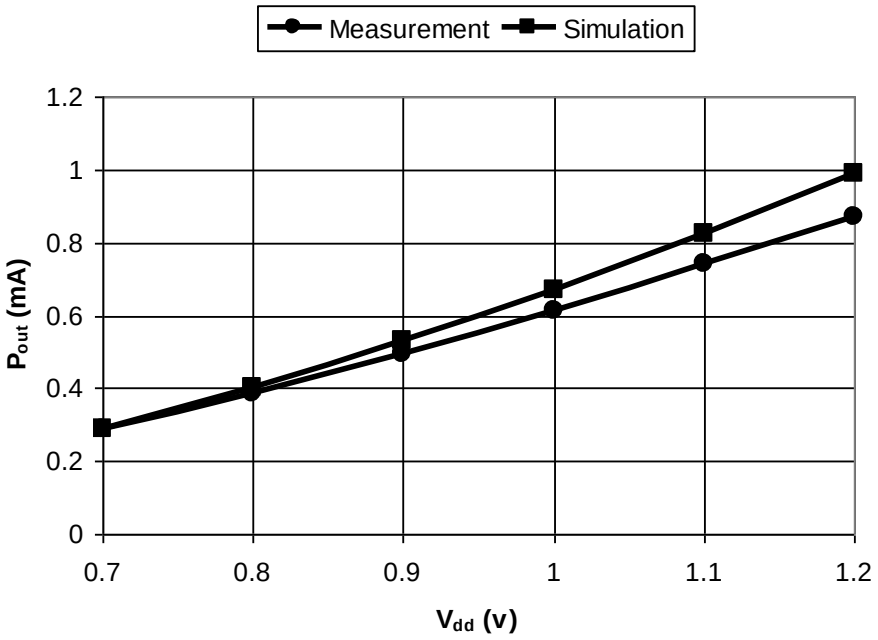


Fig. 3.12. Output power versus supply voltage.

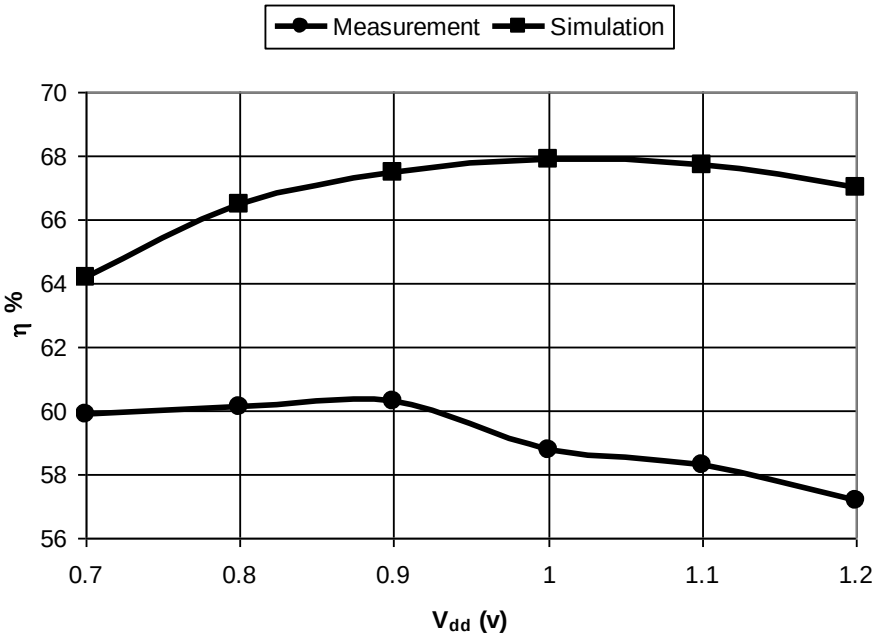


Fig. 3.13. Power amplifier efficiency versus supply voltage.

The measured frequency response of the amplifier is compared to the simulated response as illustrated in Fig. 3.14. The power amplifier efficiency at different frequencies is shown in Fig. 3.15. It is clear that there is a slight shift in the frequency response due to passive component variations.

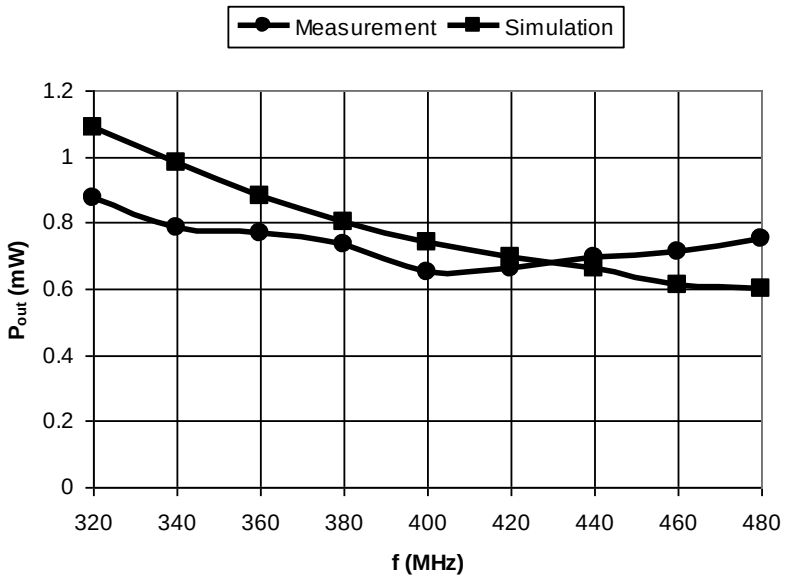


Fig. 3.14. Frequency response of power amplifier.

The power amplifier response to FSK modulated signal with frequency separation of Δf=100 KHz is shown in Fig. 3.16.

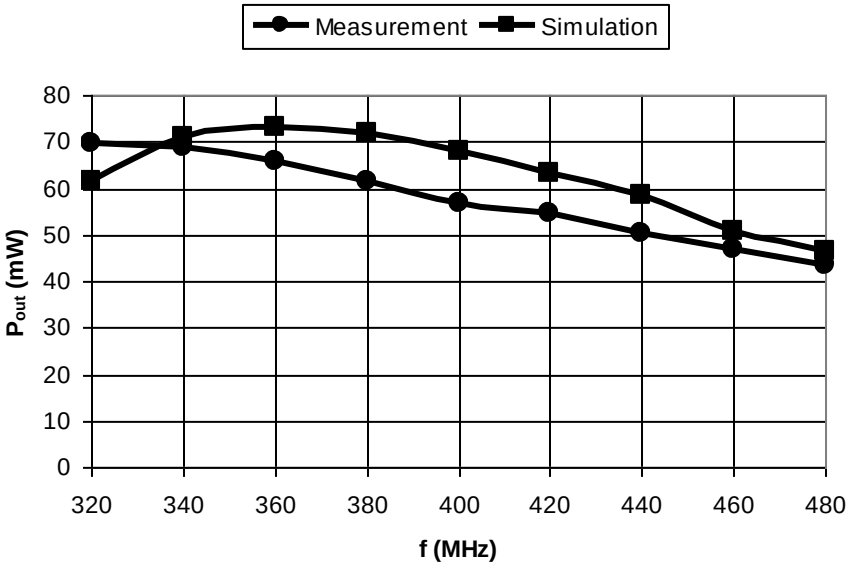


Fig. 3.15. Power amplifier efficiency at different frequencies.

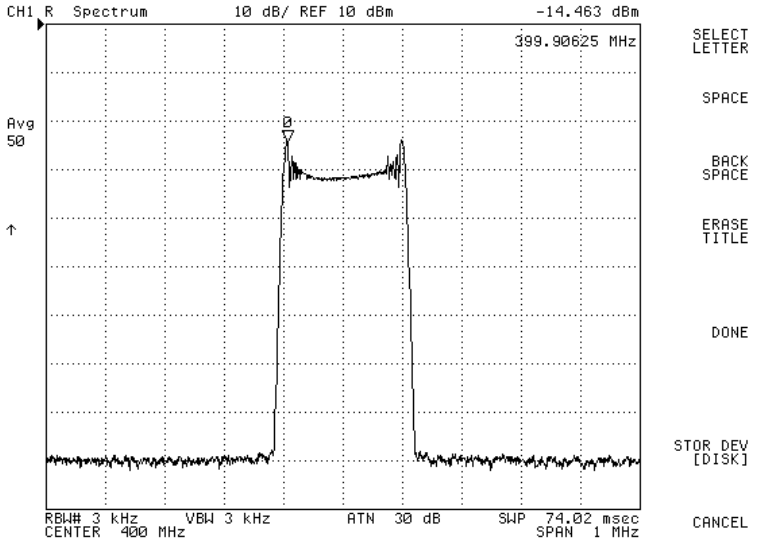


Fig. 3.16. Power amplifier output for FSK modulated signal.

CHAPTER IV

HIGH EFFICIENCY CLASS A POWER AMPLIFIER WITH DYNAMIC BIAS CONTROL

4.1 Introduction

The demand for higher data rates over wireless channels has increased significantly over the last few years. To enable transmission of large amount of data, the state of art communication systems require efficient utilization of the available bandwidth. Traditional low power communication systems employs constant envelope signals to allow the use of high efficiency switching power amplifiers. The Linearity of such switching-type amplifiers is typically very poor thus it is only suitable for low data rate applications in which constant envelope signal can be used. Envelope modulated signals are widely used nowadays as they allow the transmission of higher information rate when compared to constant envelope signals over the same channel bandwidth [50]. While constant envelope signal permit the use of the highly efficient switching power amplifiers, variable envelope signals mandate the use of less efficient but more linear power amplifier classes. Since modulated signal has average power which is typically 8-13 dB less than the peak power [50], the use of constant DC current and supply voltage to bias the power amplifier results poor efficiency at lower power levels which will lead to lower battery life in mobile transceiver systems.

The efficiency of conventional class A power amplifier can be written as [51]

$$\eta = \frac{P_o}{P_{DC}} = \frac{V_{op}^2 / 2R_L}{V_{dd} \cdot I_{DC}} = \frac{V_{op}^2}{2V_{dd}^2}, \tag{4.1}$$

where V_{op} is the peak value of output voltage, R_L is the load resistance, V_{dd} is the supply voltage and $I_{DC} = V_{dd}/R_L$ is the DC current bias. The maximum efficiency is 50% which occur when $V_{op} = V_{dd}$ and $I_{DC} = V_{dd}/R$. Since the maximum output voltage swing is limited by the supply voltage and DC current, the DC current I_{DC} and the voltage supply V_{dd} must be large enough to achieve high signal swing at signal peak power level. However, the high DC current will degrade the efficiency at the lower power levels.

There are two techniques to build highly linear PA that has an acceptable efficiency especially at low output power levels. The first technique relies on enhancing the efficiency of linear amplifiers as illustrated in Doherty amplifiers [52], while the second technique is based on linearization of non-linear amplifier.

The basic idea behind the Doherty amplifiers is to have two amplifiers, the main amplifier and an auxiliary amplifier as shown in Fig. 4.1. The main power amplifier is biased to operate at highest efficiency at the average output power and thus it has a DC current less than the required current at the maximum output power. When the input power is small enough the main PA operates in the linear mode and the auxiliary PA is turned off. As the input power increases the first PA operates in the gain-compression region and the auxiliary amplifier turns on such that it overcomes the gain compression of the main amplifier.

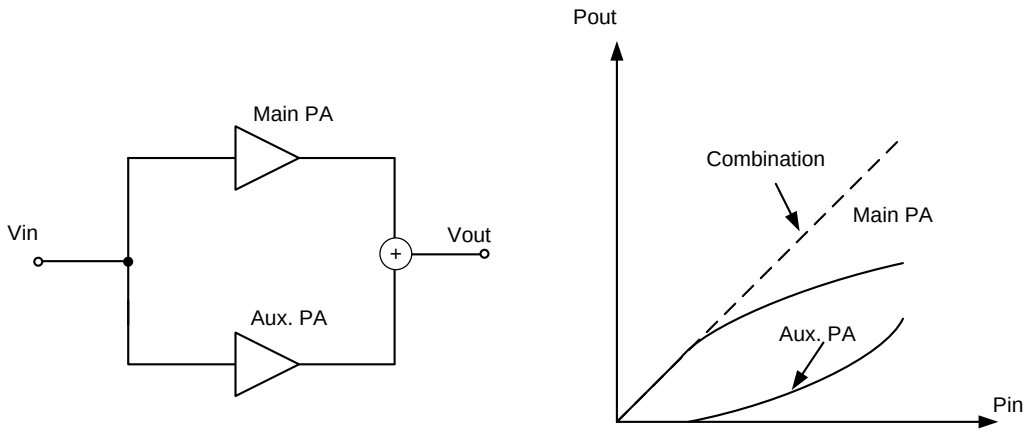


Fig. 4.1. Doherty amplifier concept.

On the other hand, the high efficiency switching power amplifier can be linearized using either outphasing or envelop elimination and restoration [48] and [53].

Fig. 4.2 displays Khan envelop elimination and restoration technique in which switching amplifier is used to achieve high efficiency. The output signal of the switching PA is proportional to the supply voltage, thus by varying the supply voltage the required amplitude modulation is achieved. In outphasing topology, the linear amplification is obtained by separating the input signal into two constant envelop signals with proper phase delay which can be amplified using switching PA and then combined again at the output as depicted in Fig. 4.3. The output in this case is given by $V_{out} = K\ cos(\Delta\varphi) \times cos(\omega_0 t)$, where $\Delta\varphi$ is the phase shift between the input signals of the power amplifiers. If the phase delay between the inputs of the two power amplifiers $\Delta\varphi$ is made proportional to the arccosine of the input signal amplitude, the output will be linearly

proportional to the input signal amplitude. However, it is still very difficult to implement low loss and high isolation power combiner at the output of two PA's [54].

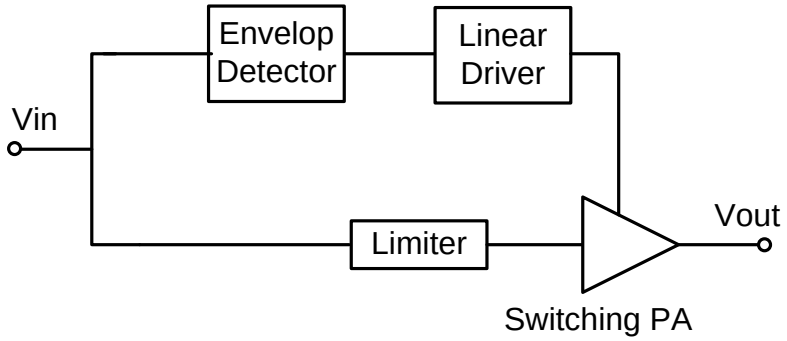


Fig. 4.2. Envelop elimination and restoration.

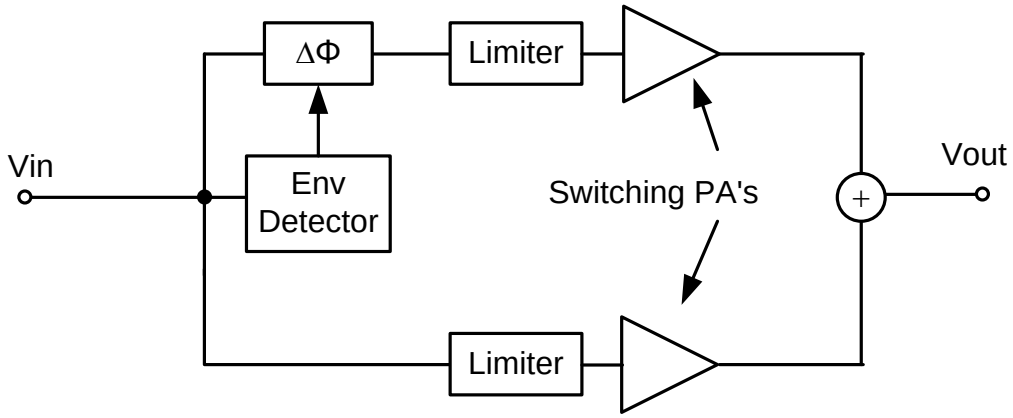


Fig. 4.3. Linear amplification using non linear amplifier (outphasing technique).

In applications where high linearity is required Class A power amplifier is typically used as it offers the best linearity among other power amplifier classes. In applications where very high linearity is required, the linearity of class A power

amplifier can be further improved using one of the following techniques: Predistortion (analog / digital), feedback, feedforward, and adaptive bias.

The Predistortion technique can be implemented in the analog or the digital domain. Analog Predistortion usually takes the form of attenuator at low signal level and no-attenuation at higher signal levels to compensate for the PA gain reduction at high signal levels. In the digital predistortion, DSP is used to compensate for the amplifier non-linearities by measuring the amplitude of the incoming signal and then apply the appropriate predistorted signal to the amplifier. It is also possible to dynamically change the correcting signal if the PA characteristics changes with time.

Feedback techniques can be categorized into direct feedback and indirect feedback. Direct feedback refers to the conventional feedback technique by taking a part of the output signal and feed it back to the input. However, the main problem is the delay between the input and the output signal which will affect the linearity improvement and the stability of the system. The indirect feedback techniques include envelope feedback, Cartesian loop and polar loops. The envelope feedback forces the output envelope of the PA to follow the input envelope as shown in Fig. 4.4. The envelope feedback however is not able to linearize the PA if it is operating in the gain compression region. The Cartesian feedback (Fig. 4.5) and polar loop uses the base-band signal information available in a complete transmitter to linearize the PA. The feedforward concept is displayed in Fig. 4.6. The basic idea is to extract the non-linear distortion at the output of the power amplifier and then subtract it from the output of the power amplifier to have a

linear output signal. Delays are added to compensate for the delays in the main PA and error amplifier.

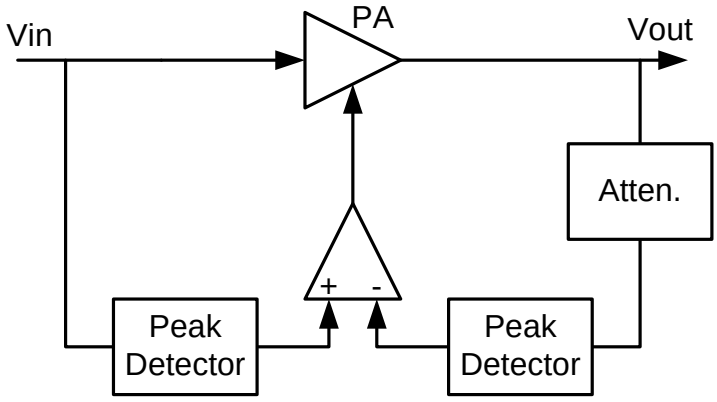


Fig. 4.4. Envelope feedback.

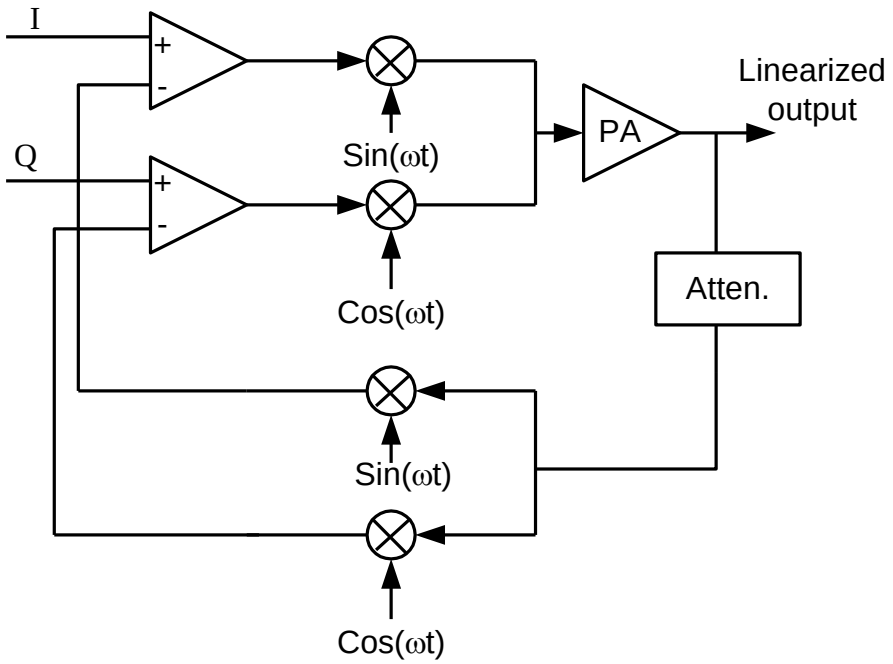


Fig. 4.5. Cartesian feedback.

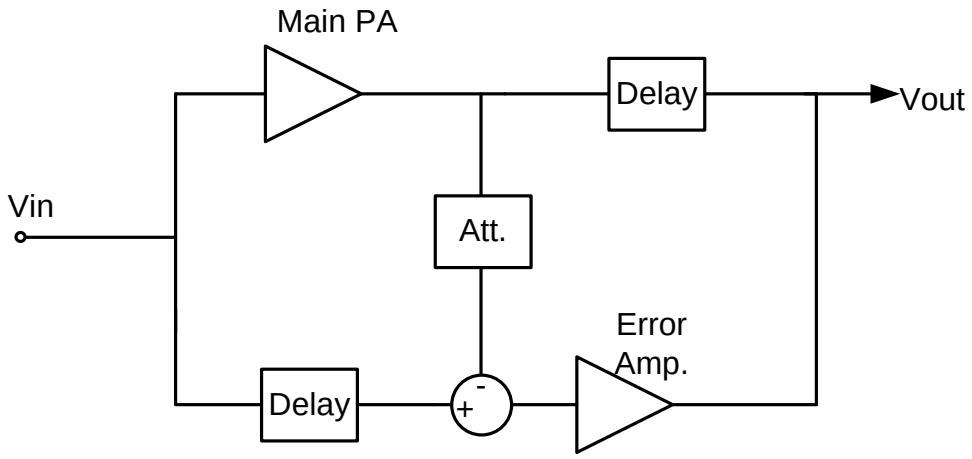


Fig. 4.6. Feedforward linearization.

The problem of gain-compression in PA can be alleviated by adjusting the bias of the PA to have higher gain. The effect of dynamic bias on the power amplifier linearity is discussed in the following section.

The efficiency of class A power amplifier is poor at low output power levels. Class A PA efficiency can be improved by dynamic adjustment of the DC current and the supply voltage with the variation of the signal envelope. For a fixed supply voltage, the optimum value of the DC current level for the highest possible efficiency is $I_{DC} = V_{op}/R_L$. In this case the efficiency is given by [51]

$$\eta = \frac{V_{op}}{2V_{dd}} \tag{4.2}$$

Changing the supply voltage dynamically will also improve the efficiency as described in [55]–[56], in which discrete levels of supply voltage are used. High

efficiency DC-DC converters can also be used to control V_{dd} in a continuous fashion [57].

As described in [55] the dynamically adjustment of the bias current enhances the linearity of the amplifier since it can be used to achieve flat gain at low and high power levels. The linearity of envelop modulated signal is typically measured using error vector magnitude (EVM), which degrades if the signal experience different gain at different power levels [58]. To achieve the maximum efficiency, the optimum DC current at a given output power level is proportional to the output voltage level ($I_{DC} = V_{op} / R_L$). However, if the bias current is made linearly proportional to the output voltage level, the linearity of the amplifier will degrade as the resulting gain of the amplifier will not be constant at different input power levels.

In this project, the current of the power amplifier is dynamically adjusted with linear dependence on the input voltage. The gain of the preamplifier is adjusted accordingly to obtain constant overall gain and consequently good linearity. The relationship between the dynamic bias behavior and the linearity of the power amplifier is presented and techniques to improve the linearity further are proposed.

4.2 Dynamic Bias of Class A Power Amplifier

The output voltage amplitude V_{om} of the power amplifier can be expressed in terms of its nonlinear coefficients and input voltage amplitude V_{im} as $V_{om} = a_1 V_{im} + 0.75 \times a_3 V_{im}^3$ [48]. Hence, the gain of the power amplifier is $G = a_1 + 0.75\, a_3\, V_{im}^2$. For negative values of a_3, the third order non-linearity of power amplifier will result in a gain

reduction as the input power increases. By using dynamic bias circuit, the DC bias current and consequently the amplifier gain should increase as the input power increases to compensate for this effect and thus result better linearity [59]-[61]. To achieve the maximum efficiency at lower output power, the DC current at low output power should be reduced to the optimum value of V_{op}/R_L. Since the gain of the amplifier is a function of the DC current, lower current will lead to lower gain at low input power levels.

In the proposed amplifier, the gain of preamplifier is increased to compensate for this gain reduction at low output power levels. At high output power levels the bias current of power amplifier is increased resulting higher gain. On other hand, the third order amplifier non-linearity causes a gain reduction as the input power increases. Hence the gain of the preamplifier should be adjusted taking into account the gain expansion due to higher DC bias current of power amplifier and the gain reduction due to non-linear behavior of the amplifier.

For a small variation in the DC gate-source voltage of MOS transistor, the DC current can be written as $I_{DC} = I_{DC0} + g_m \times \Delta V_{GS}$. Hence, the gate-source voltage V_{GS} should be made linearly proportional to signal amplitude in order to achieve the required linear DC current dependence on the output voltage. This can be easily done by using a linear envelope detector to control the gate-source voltage of the transistor. To enhance the amplifier stability, the envelope detector is placed at the input of the amplifier.

Constant gain can be translated as a linear relation between input and output signal. Thus the inter-modulation distortion should be minimal for an amplifier that exhibit constant gain at the fundamental frequency component. The following analysis

will focus on the relationship between the gain at the fundamental and the third order inter-modulation components and the effects of the dynamic bias current on distortion.

4.2.1 Dynamic Bias Effect on Amplifier Linearity

The current of MOS transistor can be approximated using Taylor series as

$$i \approx g_{m1}V_i + g_{m2}V_i^2 + g_{m3}V_i^3, \tag{4.3}$$

where g_{m1}, g_{m2} and g_{m3} are Taylor series coefficients.

The transconductance of MOS transistor is proportional to the current flowing through it and consequently the gate-source voltage V_{GS}. For a small variation of gate to source voltage ΔV_{GS}, the transconductance of the transistor can be approximated as

$$g_{m1} \approx g_{m10} + g_{m11}\Delta Vgs\,, \tag{4.4}$$

where g_{m10} is the transconductance corresponding to the gate-source DC voltage of V_{GS0}, and g_{m11} is the first order Taylor series coefficient. Equation (4.4) represents first order Taylor series expansion of transconductance as a function of the gate-source voltage V_{GS}. Similarly the following expression can be written for g_{m2}, and g_{m3}

$$\begin{aligned} g_{m2} &\approx g_{m20} + g_{m21}\Delta Vgs \\ g_{m3} &\approx g_{m30} + g_{m31}\Delta Vgs, \end{aligned} \tag{4.5}$$

For a fixed transistor bias, the output current due to two tone input voltage is composed of the fundamental components, inter-modulation components and harmonic components. The even order inter-modulation and harmonic components are widely separated from RF signal and can be easily filtered using low Q band-pass filter. Representing the two tone input in the form

$$v_i = A_m \cos((\omega_0 - \Delta\omega)t) + A_m \cos((\omega_0 + \Delta\omega)t) = 2A_m \cos(\omega_0 t)\cos(\Delta\omega t) \qquad (4.6)$$

Ignoring the even-order inter-modulation and harmonic components, the output current can be written as

$$\begin{aligned} i &\approx 2A_m g_{m1} \cos(\omega_0 t)\cos(\Delta\omega t) + 8A_m^3 g_{m3} \cos^3(\omega_0 t)\cos^3(\Delta\omega t) \\ &\approx \left(2A_m g_{m1} + \frac{9A_m^3}{2} g_{m3}\right)\cos(\omega_0 t)\cos(\Delta\omega t) \\ &+ \frac{3A_m^3}{2} g_{m3} \cos(\omega_0 t)\cos(3\Delta\omega t) + \frac{3A_m^3}{2} g_{m3} \cos(3\omega_0 t)\cos(\Delta\omega t) \\ &+ \frac{A_m^3}{2} g_{m3} \cos(3\omega_0 t)\cos(3\Delta\omega t) \end{aligned} \qquad (4.7)$$

The terms that contain third order harmonic component $3\omega_0$ will be removed by the filtering action of the output tank and can be ignored. The third order nonlinearity produced an additional term at the fundamental frequency ω_0 that cause gain compression for negative g_{m3} and inter-modulation components at frequencies $(\omega_0+3\Delta\omega)$ and $(\omega_0-3\Delta\omega)$.

As mentioned before, the current can be increased to counteract the gain reduction caused by third order non-linearity. The following analysis reveals that the dynamic adjustment of the bias current will also help to reduce third order inter-modulation components. For envelope modulated signal, the input voltage can be represented as

$$V_i = A(t)\cos(\omega_0 t), \qquad (4.8)$$

where A(t) is the time varying envelope. In the case of two tone input, the envelope is simply given by $2A_m\text{Cos}(\Delta\omega t)$. If the dynamic bias control circuit produces a bias

voltage that is proportional to the envelope of the input voltage, the DC bias current and corresponding g_m can be approximate using first order Taylor series as

$$\begin{aligned} I_{DC} &= I_{DC0} + I_{DC1}\Delta V_{GS} = I_{DC0} + I_{DC1}K_e|A(t)| \\ g_{m1} &= g_{m10} + g_{m11}\Delta V_{GS} = g_{m10} + g_{m11}K_e|A(t)| \end{aligned} \tag{4.9}$$

The absolute value function y=|x| is symmetric around x=0 and hence it can be approximated as a series of even order terms. Since the absolute value function is not differentiable at x=0, Taylor series expansion are not valid around x=0. Several optimization methods have been proposed for non differentiable functions that include numerical algorithms that overcome the problem of non-continuous derivative and approximation of the non differentiable function to a continuously differentiable function. However, the first derivative of the absolute value function changes from -1 for x<0 to 1 for x>0. Hence the conventional series approximation that is based on the derivative can't be used, instead the coefficients of the function series approximation is chosen to minimize the error between the approximation and the original function. Writing the absolute value function y=|x| using only constant term and second order term yields

$$y = |x| \approx \alpha_0 + \alpha_2 x^2 \tag{4.10}$$

For an input signal limited to –E<x<E, the coefficients α_0 and α_2 is chosen to minimize the mean square error between approximation and original function.

$$S = \int_{-E}^{E} \left(|x| - \alpha_0 - \alpha_2 x^2\right)^2 dx \tag{4.11}$$

To minimize the error, derivative relative to α_0 and α_2 should be made equal to zero

$$\begin{aligned} &\frac{\partial S}{\partial \alpha_0} = 0, \frac{\partial S}{\partial \alpha_2} = 0 \\ &\Rightarrow \alpha_0 = \frac{E}{2} - \alpha_2 \frac{E^2}{3}, \alpha_2 = \frac{5}{4E} - \frac{5}{3E^2}\alpha_0 \\ &\Rightarrow \alpha_0 = \frac{3E}{16}, \alpha_2 = \frac{15}{16E} \end{aligned} \tag{4.12}$$

Equation (4.12) reveals that the coefficients α_0 and α_2 are function of the maximum envelope signal amplitude. For a two tone input, the output of ideal envelope detector is given by

$$\begin{aligned} V_{en} &= K_e \left| 2A_m \cos(\Delta\omega t) \right| \approx \alpha_0 K_e + \alpha_2 K_e \left(2A_m \cos(\Delta\omega t) \right)^2 \\ &\approx 1.3125 A_m K_e + 0.9375 A_m K_e \cos\left(2\Delta\omega t\right) \end{aligned}, \tag{4.13}$$

where K_e is the gain of the envelope detector. In the simple case of two tone input, the spectrum of the rectified envelope $|2A_m\cos(\Delta\omega t)|$ can be obtained using Fourier series

$$2A_m \left| \cos\left(\Delta\omega t\right) \right| = 1.273 A_m + 0.85 A_m \cos\left(2\Delta\omega t\right) + \ldots \tag{4.14}$$

Comparing the approximation in (4.13) to the exact solution given by (4.14) confirms that (4.13) represents an acceptable approximation of the envelope detector output. Since the effect of the fourth order term will result in second order harmonic which has been neglected in (4.13), the exact value of the second harmonic in (4.14) is slightly different.

Using (4.9) and (4.10) g_{m1} is written in terms of the envelope amplitude

$$g_{m1} \approx g_{m10} + g_{m11}\alpha_0 K_e + g_{m11}\alpha_2 K_e A^2(t), \tag{4.15}$$

Using (4.3) and ignoring the even-order inter-modulation, the output can current can be expressed as

$$\begin{aligned} i &\approx \left(g_{m10} + g_{m11}\alpha_0 K_e + g_{m11}\alpha_2 K_e A^2(t)\right)A(t)\cos(\omega t) + g_{m3}A^3(t)\cos^3(\omega t) \\ &\approx \left(g_{m10} + g_{m11}\alpha_0 K_e\right)A(t)\cos(\omega t) + \left((3/4)g_{m3} + g_{m11}\alpha_2 K_e\right)A^3(t)\cos(\omega t) \end{aligned}, \quad (4.16)$$

where even order inter-modulation and higher order harmonics have been neglected in the approximation. In case of two-tone input, $A(t) = 2A_m\text{Cos}(\Delta\omega t)$, the output current takes the form

$$\begin{aligned} i &\approx \left(g_{m10} + g_{m11}\alpha_0 K_e\right)2A_m\cos(\Delta\omega t)\cos(\omega_0 t) \\ &+ \left((3/4)g_{m3} + g_{m11}\alpha_2 K_e\right)8A_m^3\cos^3(\Delta\omega t)\cos(\omega_0 t) \\ &= \left(g_{m10} + g_{m11}\alpha_0 K_e + \left((9/4)g_{m3} + 3g_{m11}\alpha_2 K_e\right)A_m^2\right)2A_m\cos(\Delta\omega t)\cos(\omega_0 t) \\ &+ \left((3/4)g_{m3} + g_{m11}\alpha_2 K_e\right)2A_m^3\cos(3\Delta\omega t)\cos(\omega_0 t) \end{aligned} \quad (4.17)$$

The condition to cancel third order inter-modulation components is

$$g_{m11}\alpha_2 K_e = -(3/4)g_{m3} \Rightarrow K_e = \frac{-1.6g_{m3}A_m}{g_{m11}} \quad (4.18)$$

Using (4.18), (4.17) reduces to

$$i \approx \left(g_{m10} + g_{m11}\alpha_0 K_e\right)2A_m\cos(\Delta\omega t)\cos(\omega_0 t) \quad (4.19)$$

Equation (4.19) reveals that the output consists of the fundamental component only and the third order inter-modulation has been eliminated.

The preceding analysis has been done taking into account only second order representation of the envelope detector output, a more accurate analysis can be performed using higher order representation (Fig. 4.7). The third order non-linear coefficient g_{m3} will exhibit variation as V_{GS} tracks the input envelope

$$g_{m3} \approx g_{m30} + g_{m31}\alpha_0 K_e + g_{m31}\alpha_2 K_e A^2(t), \quad (4.20)$$

In addition, more accurate representation of the absolute value function can be written taking into account up to the fourth order non-linearity

$$y = |x| \approx \alpha_0 + \alpha_2 x^2 + \alpha_4 x^4 \tag{4.21}$$

Minimizing the error function as before, the coefficients α_0, α_2, and α_4 are

$$\begin{aligned} &\alpha_0 + \alpha_2 E^2/3 + \alpha_4 E^4/5 = A/2 \\ &\alpha_0/3 + \alpha_2 E^2/5 + \alpha_4 E^4/7 = A/4 \\ &\alpha_0/5 + \alpha_2 E^2/7 + \alpha_4 E^4/9 = A/6 \\ &\Rightarrow \alpha_0 = \frac{15E}{128}, \alpha_2 = \frac{210}{128E}, \alpha_4 = \frac{-105}{128E^3} \end{aligned} \tag{4.22}$$

Using (4.22) and (4.9), g_{m1} can be written as

$$g_{m1} \approx g_{m10} + g_{m11}\alpha_0 K_e + g_{m11}\alpha_2 K_e A^2(t) + g_{m11}\alpha_4 K_e A^4(t), \tag{4.23}$$

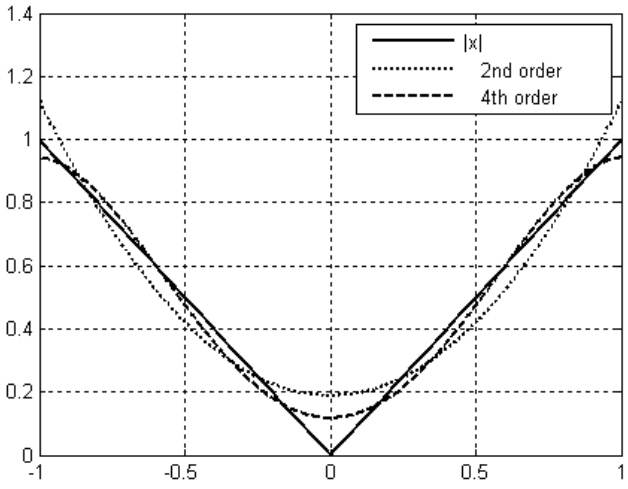


Fig. 4.7. Second and fourth order approximations of the absolute value function.

The effect of the dynamic bias on g_{m3} given by (4.20) is neglected in the following analysis and simulation results will be provided to confirm the validity of this assumption. Repeating the analysis for the output current with a two tone input signal, and using (4.16) and (4.23), the output current for a two tone input signal is expressed as

$$\begin{aligned} i &\approx \left(g_{m10}+g_{m11}\alpha_0 K_e\right)2A_m\cos(\Delta\omega t)\cos(\omega t) \\ &+\left((3/4)g_{m3}+g_{m11}\alpha_2 K_e\right)8A_m^3\cos^3(\Delta\omega t)\cos(\omega t) \\ &+32g_{m11}\alpha_4 K_e A_m^5\cos^5(\Delta\omega t)\cos(\omega t) \\ &=\left(g_{m10}+\frac{9}{4}g_{m3}A_m^2+g_{m11}K_e\left(\alpha_0+3\alpha_2 A_m^2+10\alpha_4 A_m^4\right)\right)2A_m\cos(\Delta\omega t)\cos(\omega t) \\ &+\left((3/4)g_{m3}+g_{m11}\alpha_2 K_e+5g_{m11}\alpha_4 K_e A_m^2\right)2A_m^3\cos(3\Delta\omega t)\cos(\omega t) \\ &+2g_{m11}\alpha_4 K_e A_m^5\cos(5\Delta\omega t)\cos(\omega t) \end{aligned} \tag{4.24}$$

The condition to cancel the third order harmonic in this case is given by

$$\begin{aligned} &(3/4)g_{m3}+g_{m11}\alpha_2 K_e+5g_{m11}\alpha_4 K_e A_m^2=0 \\ &\Rightarrow K_e=-\frac{256}{105}\cdot\frac{g_{m3}}{g_{m11}}A_m \end{aligned} \tag{4.25}$$

Using the condition above, the output current reduces to fundamental component and a fifth order inter-modulation product. In order to avoid having this fifth order inter-modulation product, V_{GS} control should be adjusted such that

$$V_{GS}=V_{GS0}+K_e|A(t)|+K_{e4}A^4(t)\,, \tag{4.26}$$

Repeating the analysis reveals that K_e and K_{e4} can be chosen to eliminate the third and fifth order inter-modulation products. To verify the previous analysis, a power amplifier with envelope linearization has been designed and simulated. Fig. 4.8 shows single stage power amplifier schematic in which envelope signal is used to linearize the

amplifier. Fig. 4.9 depict the third order inter-modulation of the amplifier without linearization, with $V_{GS}=V_{GS0}+K_e|A(t)|$, and with $V_{GS}=V_{GS0}+K_eA^2(t)$.

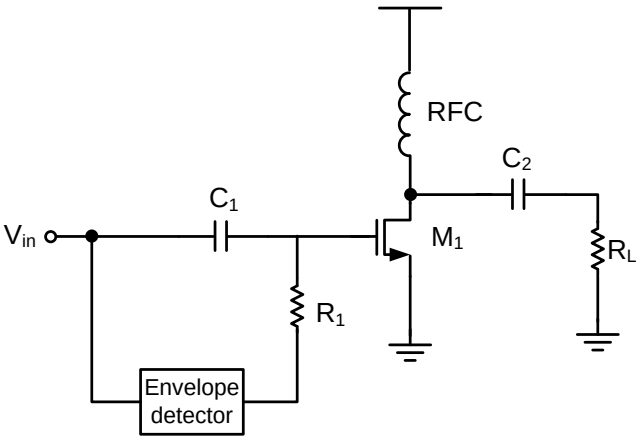


Fig. 4.8. Power amplifier linearization using envelope signal.

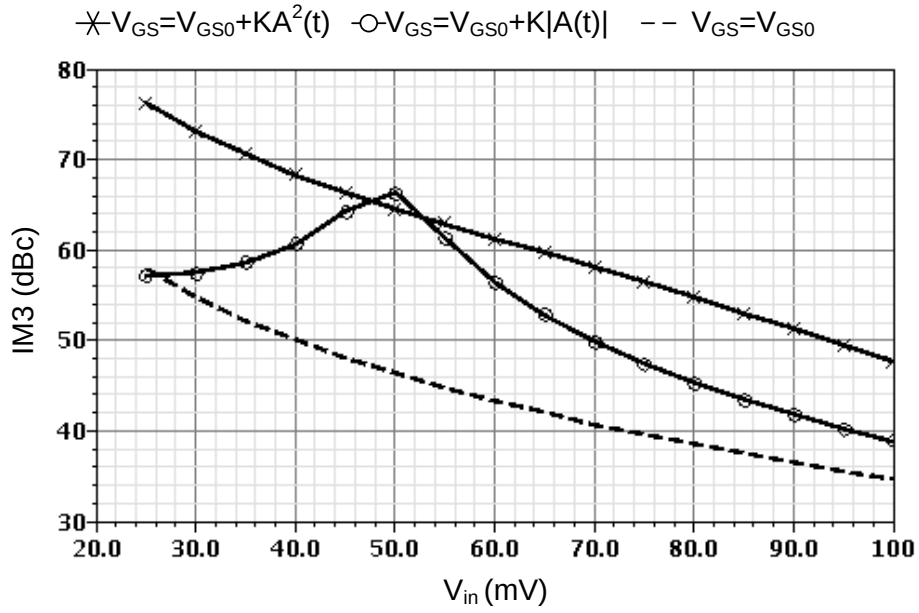


Fig. 4.9. Third order inter-modulation versus input amplitude for different control schemes.

As predicted by (4.18), the case in which V_{GS} is controlled by the envelope |A(t)| has a good IM3 performance only at a specific input amplitude. On the other hand if V_{GS} is made dependent on the square of the envelope signal, the IM3 is improved for the whole input amplitude range. Fig. 4.10 shows IM5 corresponding to different adaptive bias techniques. The fifth order inter-modulation is not much different than reference amplifier when V_{GS} is made proportional to the square of the envelope signal $A^2(t)$, which confirms the validity of the assumption that the variation in g_{m3} can be neglected. However, for the case of $V_{GS} = V_{GS0} + |A(t)|$, IM5 is degraded which can be explained by (4.24).

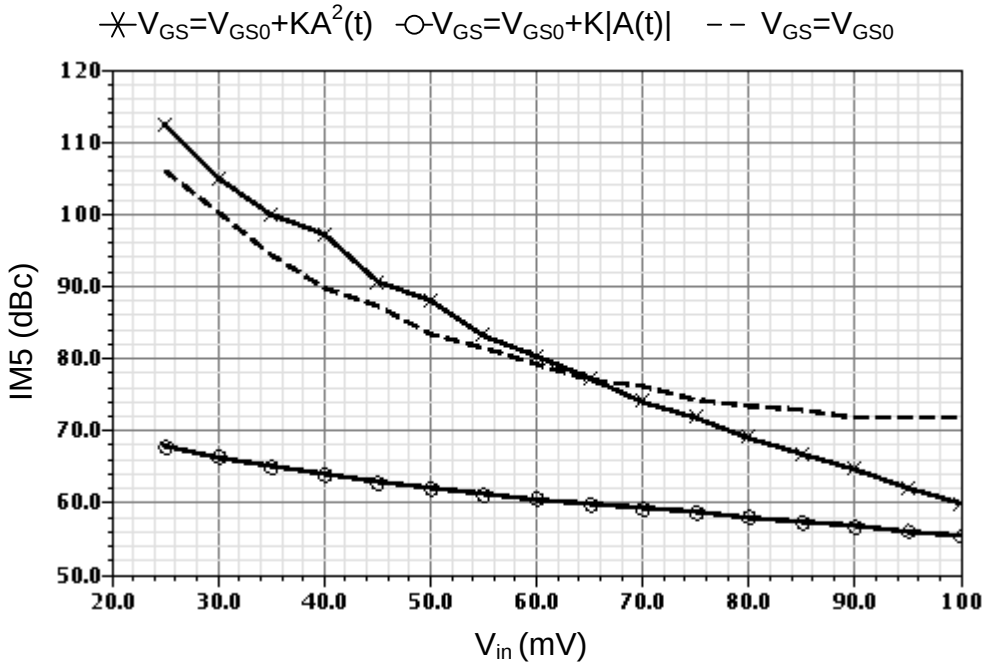


Fig. 4.10. Fifth order inter-modulation versus input amplitude for different control schemes.

As mentioned in (4.26) if $k_1A^4(t)$ is added to the adaptive transistor bias V_{GS}, The third and fifth order inter-modulation is improved as depicted in Fig. 4.11 and Fig. 4.12. The third order inter-modulation is improved over wider input range when compared to the previous case in which V_{GS} is only dependent on signal envelope.

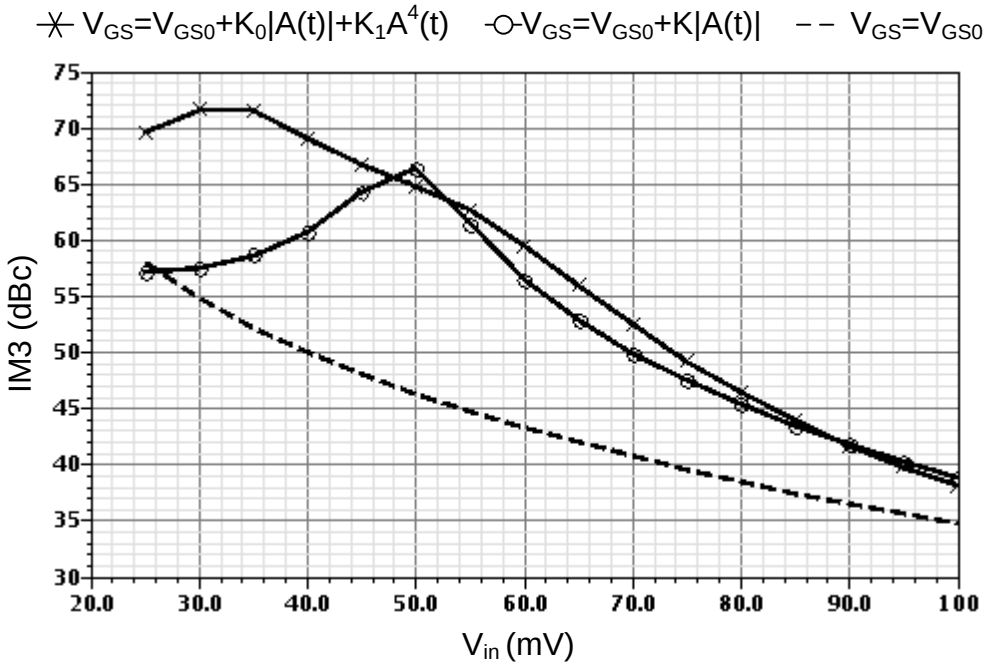


Fig. 4.11. Third order inter-modulation versus input amplitude with improved control scheme.

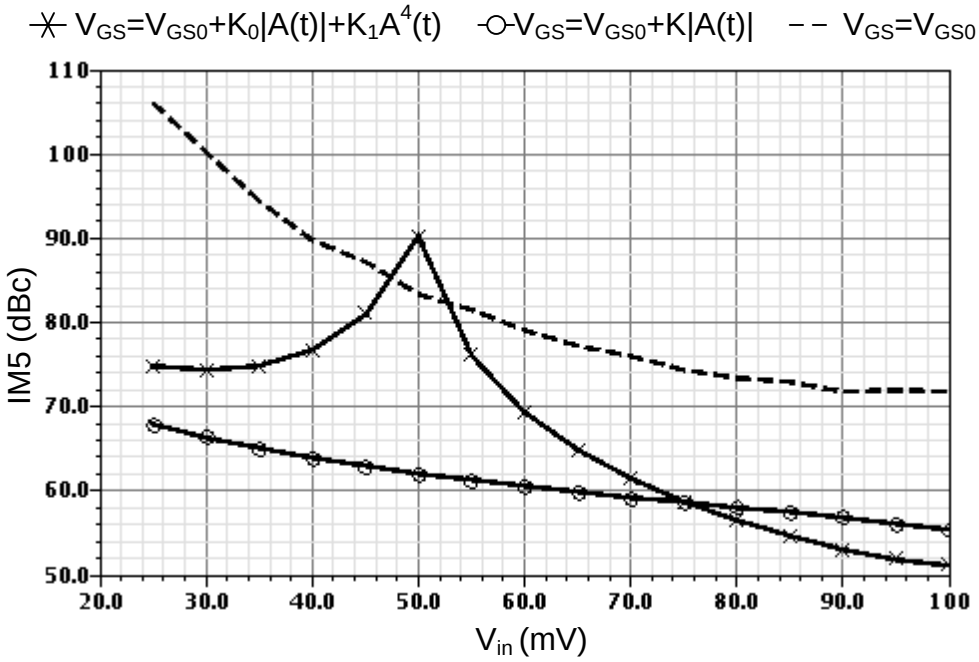


Fig. 4.12. Fifth order inter-modulation versus input amplitude with improved control scheme.

4.2.2 Efficiency Improvement Using Dynamic Bias

As mentioned before, for the best efficiency the DC current should be V_{op}/R_L. Hence the best efficiency is achieved when $V_{GS} = V_{GS0} + K_e |A(t)|$, where K_e is chosen such that I_{DC} is linearly proportional to the output voltage amplitude. Section 4.2.1 shows that K_e can be chosen to cancel the effect of third order non-linearity and since third order non-linear coefficient a_3 is typically small, the required K_e is typically small. In other words, the bias current should be slightly increased to counteract the gain reduction caused by non-linearities. However, the required K_e for good efficiency is much higher, which will be translated into higher gain variations and higher third order

inter-modulation and thus poor error vector magnitude (EVM). The proposed solution to overcome this problem is to adjust the gain of the preamplifier to have a flat gain and to reduce the inter-modulation components. As shown in Fig. 4.13, the bias of the preamplifier is also made dependent on the signal envelope.

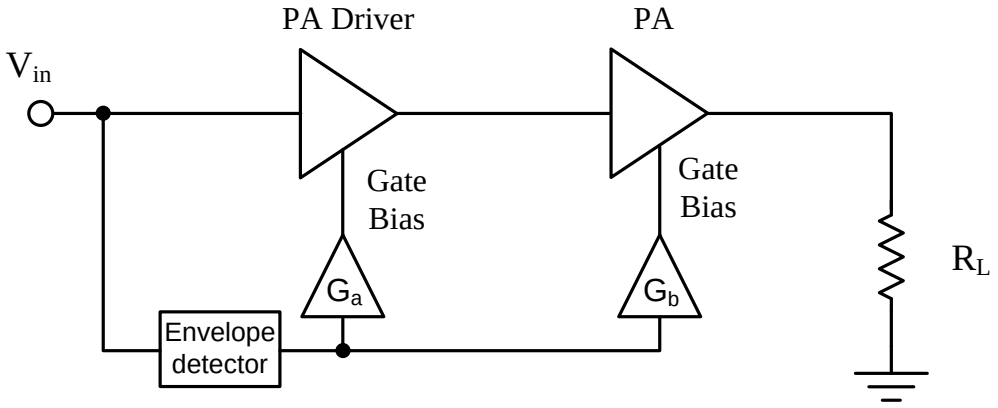


Fig. 4.13. Efficiency enhancement through dynamic bias of power amplifier.

Assuming that the envelope detector has a gain of unity, the gate-source voltage, DC current, and transconductance of the preamplifier can be written as

$$\begin{aligned} V_{GS}^{a} &= V_{GS0}^{a} + \Delta V_{GS0}^{a} = V_{GS0}^{a} + G_a|A(t)| \\ I_{DC}^{a} &= I_{DC0}^{a} + I_{DC1}^{a}\Delta V_{GS0}^{a} = I_{DC0}^{a} + I_{DC1}^{a}G_a|A(t)| \\ g_{m1}^{a} &= g_{m10}^{a} + g_{m11}^{a}\Delta V_{GS0}^{a} = g_{m10}^{a} + g_{m11}^{a}G_a|A(t)| \end{aligned} \tag{4.27}$$

Similarly, the gate-source voltage, DC current, and transconductance of the main amplifier are given by

$$\begin{aligned} V_{GS}^{b} &= V_{GS0}^{b} + \Delta V_{GS0}^{b} = V_{GS0}^{b} + G_b|A(t)| \\ I_{DC}^{b} &= I_{DC0}^{b} + I_{DC1}^{b}\Delta V_{GS0}^{b} = I_{DC0}^{b} + I_{DC1}^{b}G_b|A(t)| \\ g_{m1}^{b} &= g_{m10}^{b} + g_{m11}^{b}\Delta V_{GS0}^{b} = g_{m10}^{b} + g_{m11}^{b}G_b|A(t)| \end{aligned} \tag{4.28}$$

Ignoring the even order distortion and using the absolute value second order approximation given by (4.10), the output voltage of the pre-amplifier V_{oa} takes the form

$$\begin{aligned} V_{oa} \approx & \left(g_{m10}^{a} + g_{m11}^{a}\alpha_0 G_a\right)A(t)\cos(\omega t)R_{L1} \\ & + \left((3/4)g_{m3}^{a} + g_{m11}^{a}\alpha_2 G_a\right)R_{L1}A^3(t)\cos(\omega t) \end{aligned} \tag{4.29}$$

The output voltage of the power amplifier V_o is given by

$$\begin{aligned} V_o &\approx g_{m1}^{b}R_L V_{oa} + g_{m3}^{b}R_L V_{oa}^3 = g_{m1}^{b}R_L\left(g_{m1}^{a}R_{L1}V_{in} + g_{m3}^{a}R_{L1}V_{in}^3\right) \\ &\quad + g_{m3}^{b}R_L\left(g_{m1}^{a}R_{L1}V_{in} + g_{m3}^{a}R_{L1}V_{in}^3\right)^3 \\ &\approx g_{m1}^{b}g_{m1}^{a}R_L R_{L1}V_{in} + g_{m1}^{b}R_L g_{m3}^{a}R_{L1}V_{in}^3 + g_{m3}^{b}R_L\left(g_{m1}^{a}R_{L1}\right)^3 V_{in}^3 \end{aligned} \tag{4.30}$$

As mentioned before, for the best efficiency, the current should be highly dependent on the input envelope, which will lead to a strong non-linear behavior. In order to minimize third order inter-modulation caused by the dynamic bias, $g_{m1}^{a}g_{m1}^{b}$ should be approximately constant for any input level. In fact, a small second order dependence on the input amplitude will help to compensate for the third order non-linearity of the transistor. Using (4.27) and (4.28), $g_{m1}^{a}g_{m1}^{b}$ can be approximated as

$$\begin{aligned} g_{m1}^{a}g_{m1}^{b} \approx & \left(g_{m10}^{b} + g_{m11}^{b}\alpha_0 G_b\right)\left(g_{m10}^{a} + g_{m11}^{a}\alpha_0 G_a\right) \\ & + \left[\left(g_{m10}^{b} + g_{m11}^{b}\alpha_0 G_b\right)g_{m11}^{a}\alpha_2 G_a + \left(g_{m10}^{a} + g_{m11}^{a}\alpha_0 G_a\right)g_{m11}^{b}\alpha_2 G_b\right]A^2(t) \\ & + g_{m11}^{a}\alpha_2 G_a g_{m11}^{b}\alpha_2 G_b A^4(t) \end{aligned} \tag{4.31}$$

Following the analysis given in section 4.2.1, the third order inter-modulation is minimized when gain dependence on the square of the signal envelope is eliminated.

$$\left[\left(g_{m10}^{b}+g_{m11}^{b}\alpha_0 G_b\right)g_{m11}^{a}\alpha_2 G_a+\left(g_{m10}^{a}+g_{m11}^{a}\alpha_0 G_a\right)g_{m11}^{b}\alpha_2 G_b\right]A^2(t)=0$$
$$\Rightarrow G_b \approx -\frac{g_{m11}^{a}g_{m10}^{b}}{g_{m11}^{b}g_{m10}^{a}}G_a \ \ for\ small\ \alpha_0 \tag{4.32}$$

The forth order dependence on the envelope in (4.31) will create unwanted fifth order inter-modulation products. In order to overcome transistor intrinsic non-linearities, the value of G_b should be chosen slightly different than the value given in (4.32) to create a small amount of third order distortion that cancels third order distortion due to g_{m3}. To overcome the unwanted fifth order inter-modulation products, the bias voltage of the main power amplifier should take the form $V_{GS}^{b}=V_{GS0}^{b}+G_a|A(t)|+G_{a4}A^4(t)$.

4.3 Power Amplifier Circuit Implementation

To verify the proposed efficiency enhancement technique, a test chip was fabricated in UMC 90nm. The power amplifier is designed to drive a 50Ω load, with maximum output power of about 10dBm using a supply voltage of 1.2V. The DC current at the maximum output power is given by $V_{op}/R_L \approx 20$ mA. Using the proposed technique, the current is made linearly proportional to the input envelope. The complete PA diagram is depicted in Fig. 4.14 where RF chokes were replaced by LC tanks which help to filter the even order inter-modulation as well as signal harmonics.

Coupling caps C_{c1} and C_{c2} and bias resistors R_1 and R_2 act as a high pass filter for the RF signal, and as a low pass signal for the bias voltage. Since the bias voltage is proportional to the signal envelope, it can be approximated as a series that contains even order terms. Hence the bias voltage consists of the even order harmonics of the envelope

and the cutoff of the bias network should be larger than maximum harmonic order needed to linearize the amplifier. Since the previous analysis shows that fourth order series represents a good approximation of bias voltage dependence on input envelope, the cut off frequency should be larger than 4 times the envelope bandwidth. The constrain on the bias network cutoff can be written as

$$4\times(2\pi f_{env})<1/R_{1,2}C_{c1,2}<2\pi f_0 \tag{4.33}$$

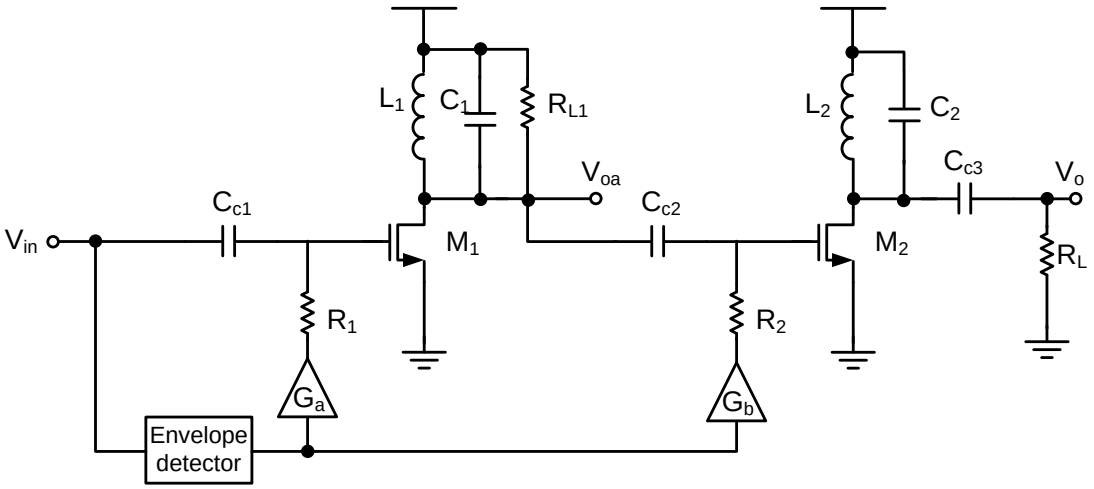


Fig. 4.14. Power amplifier schematic.

4.3.1 Envelope Detector Design

The envelope detector circuit shown in Fig. 4.15 is used to extract the signal envelope from the RF signal. The transistor M1 acts as a diode which is connected to the envelope detector cap C_2. Resistor R_1 and capacitor C_1 constitute DC decoupling circuit to enable adjustment of DC bias for proper operation of the envelope circuit. A replica of the envelope detection branch is used together with an operational amplifier in order to

eliminate non-linear effects caused by M_1 variable gate-source voltage [62]. Since the envelope signal is usually limited to one or several megahertz range, the bias current of the envelope detector can be made very small. The bias currents I_{b1} and I_{b2} are chosen to be 20 μA, while achieving g_{m1}, $g_{m2} \approx 0.6$mA/V. The envelope detector capacitor is chosen to be 5 PF. The operational amplifier design used in the envelope detector and the gain blocks in Fig. 4.14 is discussed in the following section.

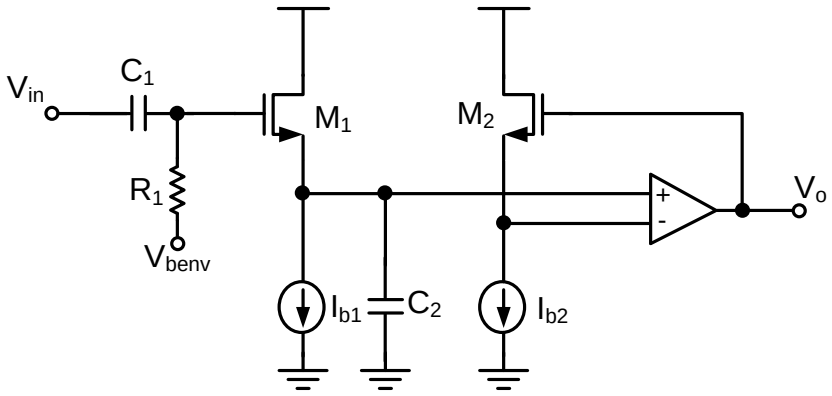
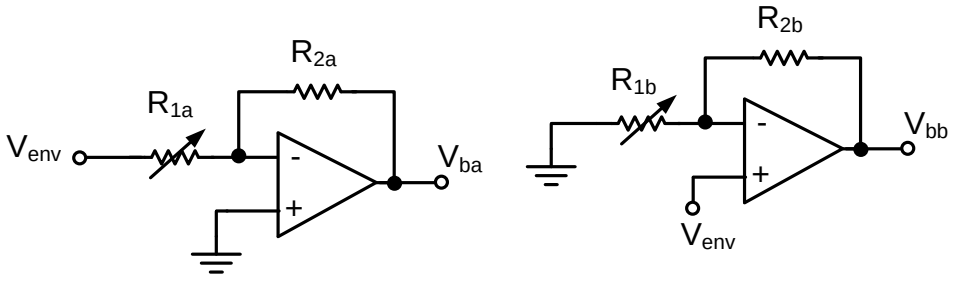


Fig. 4.15. Envelope detector schematic.

4.3.2 Operational Amplifier Design

The bias voltage of the power amplifier increases as the input voltage increases, hence the gain block G_b in Fig. 4.14 should be positive. On the other hand, the preamplifier bias should decrease as the input signal increases and thus G_a should be a negative gain block. Since the linearity of these gain blocks are very important, feedback inverting and non-inverting amplifiers shown in Fig. 4.16 are used.

The same operational amplifier is used in the envelope detector as well as dynamic bias control circuits. In order to achieve high efficiency, the power consumption of the op-amp should be minimized while the gain of the op-amp should be high enough to achieve good linearity.



(a)

(b)

Fig. 4.16. Dynamic bias amplifiers: (a) Gain stage of preamplifier (G_a). (b) Gain stage of power amplifier (G_b).

The two stage op-amp visualized in Fig. 4.17 offer high gain and low power consumption for low GBW. The bias transistors M_5 and M_6 are biased at 100μA and 50μA respectively. Miller compensation capacitor C_c is used to achieve good phase margin, and the resistor R_c is used to eliminate right hand plane zero as explained in [63]. The operational amplifier DC gain is around 51 dB and GBW is about 850MHz with phase margin of 85° as shown in Fig. 4.18.

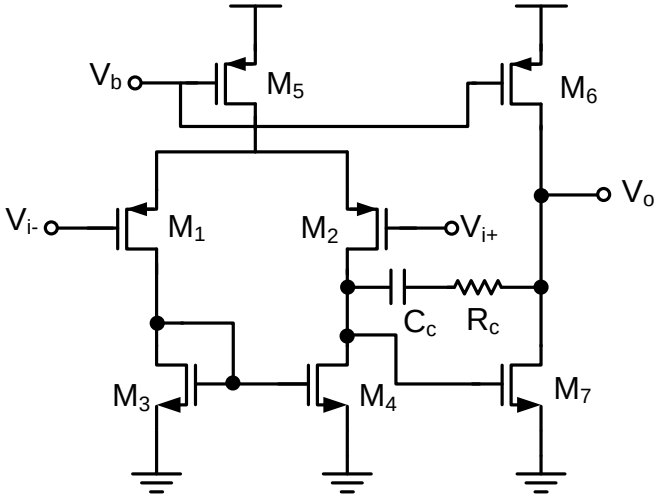


Fig. 4.17.Two stage op-amp schematic.

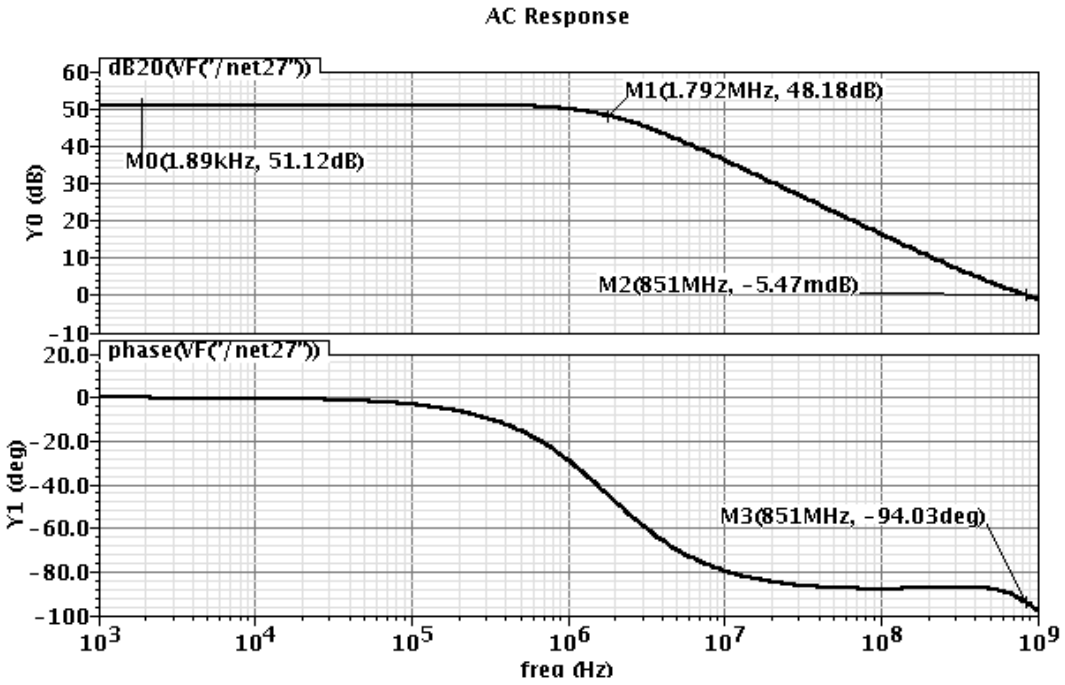


Fig. 4.18. Frequency response of the operational amplifier.

4.4 Experimental Results

The test chip was fabricated in UMC 90nm and it occupies about 0.25 mm^2 of active area. Chip micrograph is shown in Fig. 4.19. The power amplifier gain and linearity is measured at 400 MHz.

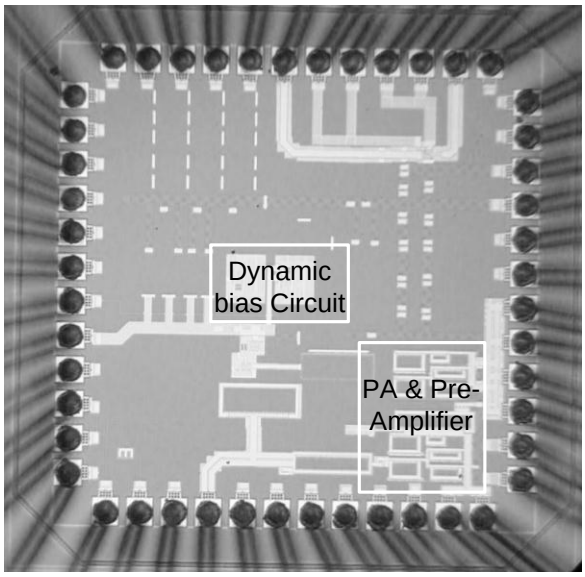


Fig. 4.19. Power amplifier chip micrograph.

Resistors R_{1a} and R_{1b} in Fig. 4.16 are made variable with 4 bit control accuracy to set the gain of the dynamic bias of both the pre-amplifier and the main power amplifier. By switching the gain of the pre-amplifier dynamic bias control circuit to zero, the reference power amplifier can be characterized without the proposed efficiency enhancement technique. The bias current of main power amplifier in this case does increase slightly as the input power increases to compensate for the gain compression caused by third order transistor non-linearities as explained in section 4.2.1. The gain of

the amplifier versus input power is shown in Fig. 4.20 with small signal gain of around 20 dB. The output 1 dB compression point P_{1dB} is about 9.2 dBm.

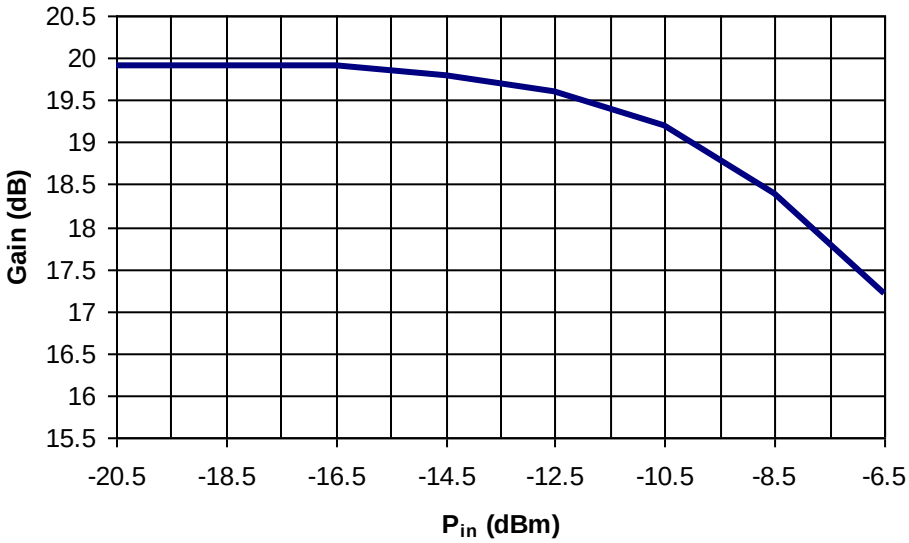


Fig. 4.20. Gain of the reference power amplifier.

If the bias of the output power amplifier is made dependent on the signal envelope while leaving the preamplifier bias fixed, the gain will exhibit expansion as the input power increases as shown in Fig. 4.21.

While the efficiency does improve, the EVM of such amplifier will be very poor due to different gain at different input power levels. By employing the dynamic bias control at both the pre-amplifier and the main power amplifier, the effect of this gain expansion can be eliminated as shown in Fig. 4.22.

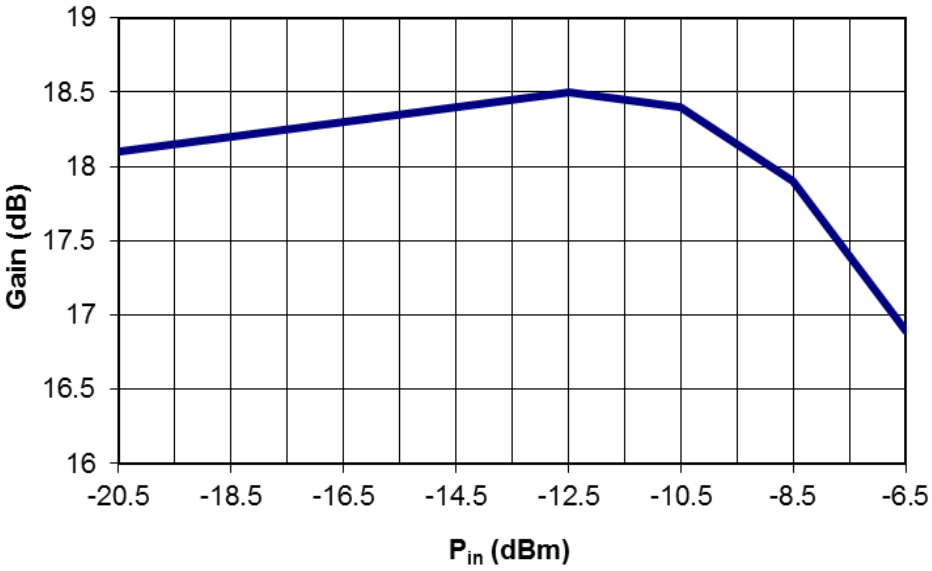


Fig. 4.21. Gain of the power amplifier with dynamic bias only at the output stage.

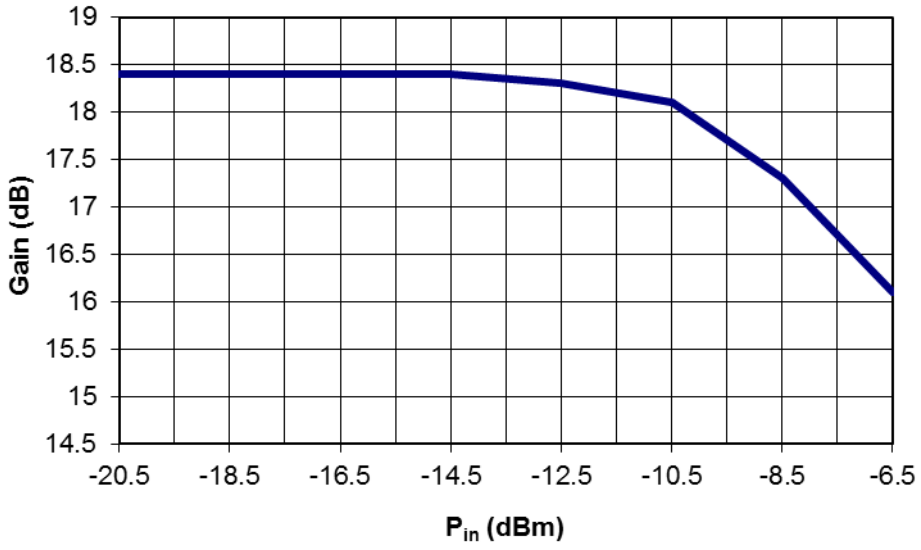


Fig. 4.22. Gain of the proposed dynamically biased power amplifier.

The output 1dB compression point in this case is around 8.7 dBm, which is slightly less than the reference case of fixed bias power amplifier. This small reduction is due to the non-linear relationship between transconductance and V_{GS}. In other word, at higher input signal levels, the gain of preamplifier is reduced more than the increase in the gain of the main PA causing this slight reduction in 1dB compression point. The efficiency of the proposed technique is higher than the efficiency of the reference power amplifier as illustrated in Fig. 4.23. The power consumption of both amplifiers is shown in Fig. 4.24. As mentioned before, if the dynamic bias is applied only to the output stage, the gain will exhibit expansion and the inter-modulation components will be higher than the reference amplifier.

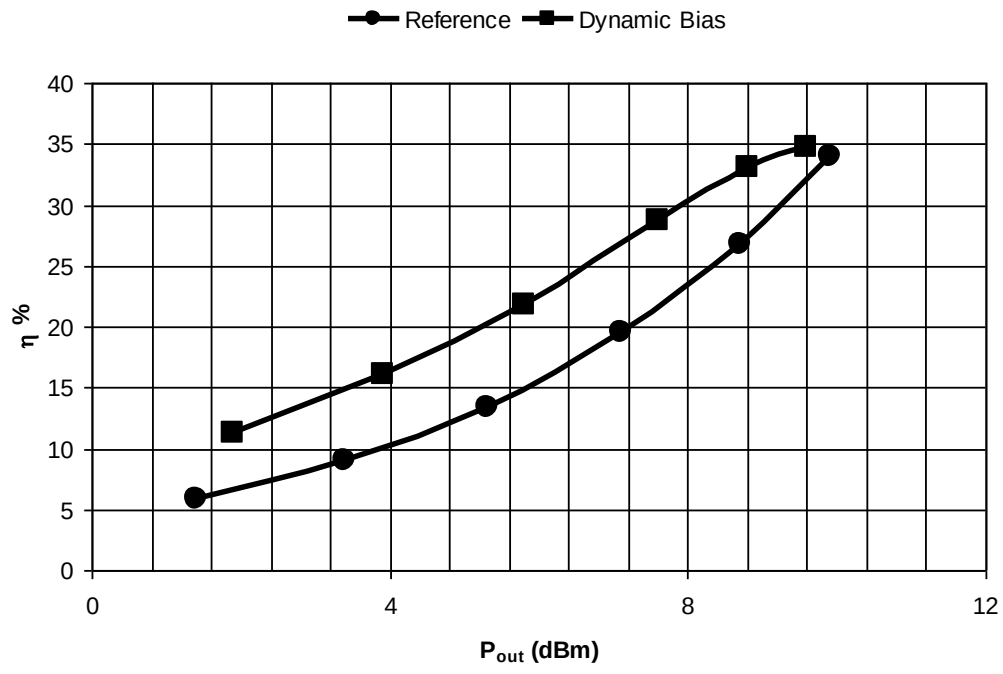


Fig. 4.23. Efficiency of the proposed dynamic bias amplifier and the reference amplifier.

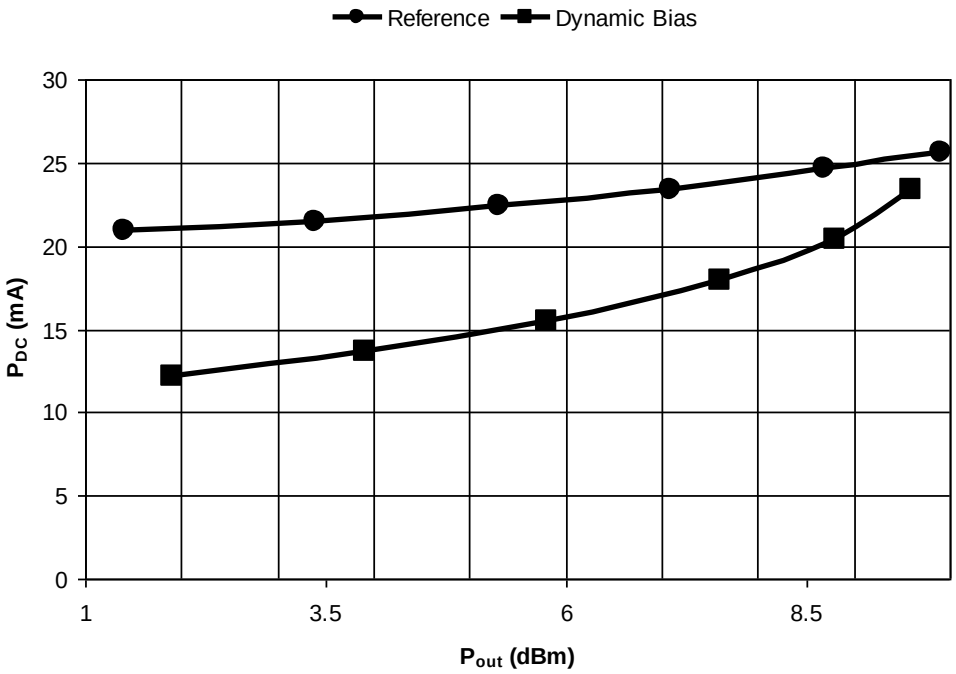


Fig. 4.24. Power consumption of the proposed dynamic bias amplifier and the reference amplifier.

The third order and fifth order inter-modulation components of the proposed dynamic bias amplifier, the reference amplifier and the amplifier with a fixed bias pre-amplifier are displayed in Fig. 4.25 and 4.26 respectively.

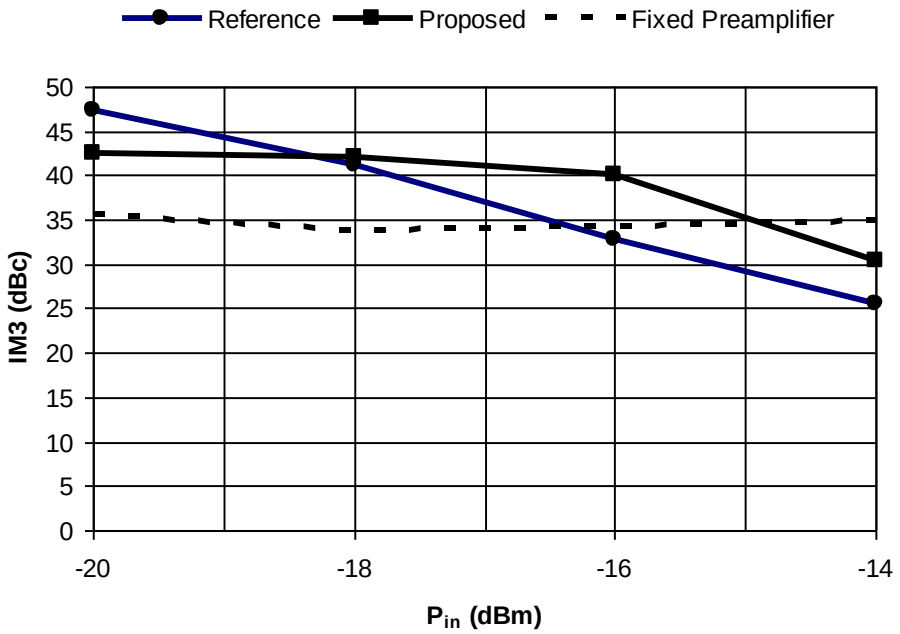


Fig. 4.25. Third order inter-modulation of the proposed and the reference amplifiers.

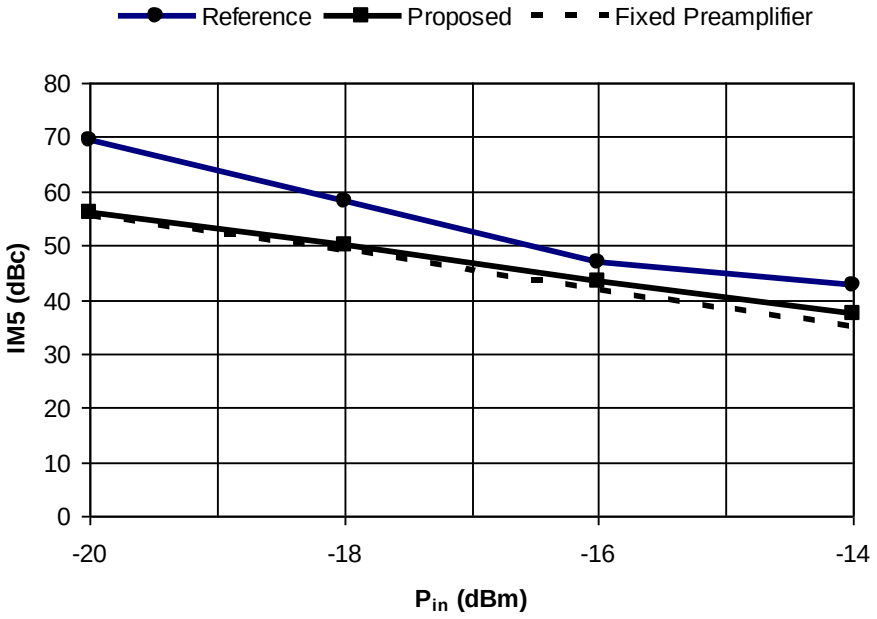


Fig. 4.26. Fifth order inter-modulation of the proposed and the reference amplifiers.

The gain of the dynamic bias control circuit can be adjusted to achieve flat overall gain and to cancel the effects of transistor non-linearities such that the third order inter-modulation component of the proposed amplifier is better that the reference amplifier at high output power levels as seen in Fig. 4.25. The proposed amplifier has higher third order inter-modulation component than the reference amplifier at lower power levels. This is due to the fact that the transconductance has been modeled as a linear function of the bias voltage V_{GS}, however this is not accurate over a wide range of the input voltage and other non-linearities must be included in order to get more accurate results.

Moreover, the fifth order inter-modulation of the proposed amplifier is higher than the reference amplifier which is attributed to the forth order term in (4.31) that is not corrected by using a linear bias control scheme. To achieve better performance at lower power levels and to solve the problem of high fifth order inter-modulation, non-linear control should be implemented in the dynamic bias circuit as illustrated in section 4.2.1. The advantage of proposed technique over conventional predistortion techniques is that the envelope frequency is relatively low and thus low speed ADC and DSP can be used to linearize the power amplifier.

CHAPTER V

CONCLUSIONS

An attenuation-predistortion technique was proposed to linearize transconductance amplifiers in Gm-C filter applications over a wide frequency range and across PVT variations. The high-frequency linearity enhancement is based on Volterra series analysis. Experimental results confirm the efficacy of the OTA linearization at high frequencies to obtain IM3 as low as -74dB with 0.2Vinp-p at 350MHz. Measurements of a biquad demonstrated that the linearization methodology is suitable for Gm-C filter applications requiring an overall IM3 $\leq$ -70dB up to the cutoff frequency. The proposed linearization approach is independent of the OTA architecture and robust due to the use of matched OTAs to cancel output distortion, resulting in an IM3 improvement of up to 22dB. Compensation for PVT variations and high-frequency effects is based on digital adjustment of resistors without changing the bias conditions, which would affect other design parameters. Hence, the main OTA can be optimized for its target application. Higher frequency operation of the proposed low pass filter is possible if other parasitic poles are taken into account. Volterra series analysis can be extended to include the second order effects due to internal parasistic pole of OTA. By modifying the frequency compensation block to match the delay of the second order parasitic poles, higher linearization bandwidth can be obtained.

High efficiency class D power amplifier has been implemented for applications that require low power consumption and low data rate transmission with constant

envelope signals. Design methodology of high efficiency power amplifier at low output power level was presented and verified with experimental results. The amplifier operates at 400MHz with output power of -2dBm and efficiency close to 60%. The output power and the efficiency have been given at different supply voltage and at different frequencies which demonstrate the high efficiency operation for different power levels. The amplifier operation with FSK modulated input signal is illustrated where low out of band spectral content is obtained.

The analysis of dynamic bias effect on efficiency and linearity of power amplifier has been presented. A dynamically biased class A power amplifier suitable for the transmission of envelope modulated signals has been fabricated. Measurement results shows that the proposed amplifier has about 18.5 dB of gain and efficiency up to 35% at 400MHz and IM3 as low as 30dB at -14 dBm of input power. Compared to the reference amplifier without dynamic bias control, the IM3 is improved for high input levels and the efficiency is improved at low output power levels. Hence the overall efficiency is enhanced for envelope modulated signals which typically has peak to average power ratio of 6dB or more. The bias control design was based on the approximation that the transconductance vary linearly with the gate-source voltage of the transistor. Higher linearity is possible using advanced DSP to control the bias current of the power amplifier while taking into account the transconductance non-linearities and the transistor output resistance non-linearities. It is also possible to add even order nonlinear terms to the bias control network to allow more degrees of freedom that will result better control of the distortion cancellation.

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